

[illegible][illegible][illegible][illegible][illegible]

TI CONFIDENTIAL - NDA RESTRICTIONS

U52-7	mcasp1_aclkr/mcasp7_axr2/vout2_d0/vin4a_d0/i2c4_sda/gpio5_0
	mcasp1_aclkx/vin6a_fld0/i2c3_sda/gpio7_31
	mcasp1_fsr/mcasp7_axr3/vout2_d1/vin4a_d1/i2c4_scl/gpio5_1
	mcasp1_fsx/vin6a_de0/i2c3_scl/gpio7_30
	mcasp1_axr0/uart6_rxd/vin6a_vsync0/i2c5_sda/gpio5_2
	mcasp1_axr1/uart6_txd/vin6a_hsync0/i2c5_scl/gpio5_3
	mcasp1_axr2/mcasp6_axr2/uart6_ctsn/vout2_d2/vin4a_d2/gpio5_4
	mcasp1_axr3/mcasp6_axr3/uart6_rtsn/vout2_d3/vin4a_d3/gpio5_5
	mcasp1_axr4/mcasp4_axr2/vout2_d4/vin4a_d4/gpio5_6
	mcasp1_axr5/mcasp4_axr3/vout2_d5/vin4a_d5/gpio5_7
	mcasp1_axr6/mcasp5_axr2/vout2_d6/vin4a_d6/gpio5_8
	mcasp1_axr7/mcasp5_axr3/vout2_d7/vin4a_d7/timer4/gpio5_9
	mcasp1_axr8/mcasp6_axr0/spi3_sclk/vin6a_d15/timer5/gpio5_10
	mcasp1_axr9/mcasp6_axr1/spi3_d1/vin6a_d14/timer6/gpio5_11
	mcasp1_axr10/mcasp6_aclkx/mcasp6_aclkr/spi3_d0/vin6a_d13/timer7/gpio5_12
	mcasp1_axr11/mcasp6_fsx/mcasp6_fsr/spi3_cs0/vin6a_d12/timer8/gpio4_17
	mcasp1_axr12/mcasp7_axr0/spi3_cs1/vin6a_d11/timer9/gpio4_18
	mcasp1_axr13/mcasp7_axr1/vin6a_d10/timer10/gpio6_4
	mcasp1_axr14/mcasp7_aclkx/mcasp7_aclkr/vin6a_d9/timer11/gpio6_5
	mcasp1_axr15/mcasp7_fsx/mcasp7_fsr/vin6a_d8/timer12/gpio6_6
	mcasp2_aclkr/mcasp8_axr2/vout2_d8/vin4a_d8
	mcasp2_aclkx/vin6a_d7
	mcasp2_fsr/mcasp8_axr3/vout2_d9/vin4a_d9
	mcasp2_fsx/vin6a_d6
	mcasp2_axr0/vout2_d10/vin4a_d10
	mcasp2_axr1/vout2_d11/vin4a_d11
	mcasp2_axr2/mcasp3_axr2/vin6a_d5/gpio6_8
	mcasp2_axr3/mcasp3_axr3/vin6a_d4/gpio6_9
	mcasp2_axr4/mcasp8_axr0/vout2_d12/vin4a_d12/gpio1_4
	mcasp2_axr5/mcasp8_axr1/vout2_d13/vin4a_d13/gpio6_7
	mcasp2_axr6/mcasp8_aclkx/mcasp8_aclkr/vout2_d14/vin4a_d14/gpio2_29
	mcasp2_axr7/mcasp8_fsx/mcasp8_fsr/vout2_d15/vin4a_d15/gpio1_5
	mcasp3_aclkx/mcasp3_aclkr/mcasp2_axr12/uart7_rxd/vin6a_d3/gpio5_13
	mcasp3_fsx/mcasp3_fsr/mcasp2_axr13/uart7_txd/vin6a_d2/gpio5_14
	mcasp3_axr0/mcasp2_axr14/uart7_ctsn/uart5_rxd/vin6a_d1
	mcasp3_axr1/mcasp2_axr15/uart7_rtsn/uart5_txd/vin6a_d0/vin5a_fld0
	mcasp4_aclkx/mcasp4_aclkr/spi3_sclk/uart8_rxd/i2c4_sda/vout2_d16/vin4a_d16/vin5a_d15
	mcasp4_fsx/mcasp4_fsr/spi3_d1/uart8_txd/i2c4_scl/vout2_d17/vin4a_d17/vin5a_d14
	mcasp4_axr0/spi3_d0/uart8_ctsn/uart4_rxd/vout2_d18/vin4a_d18/vin5a_d13
	mcasp4_axr1/spi3_cs0/uart8_rtsn/uart4_txd/vout2_d19/vin4a_d19/vin5a_d12
	mcasp5_aclkx/mcasp5_aclkr/spi4_sclk/uart9_rxd/i2c5_sda/mlb_clk/vout2_d20/vin4a_d20/vin5a_d11
	mcasp5_fsx/mcasp5_fsr/spi4_d1/uart9_txd/i2c5_scl/vout2_d21/vin4a_d21/vin5a_d10
	mcasp5_axr0/spi4_d0/uart9_ctsn/uart3_rxd/mlb_sig/vout2_d22/vin4a_d22/vin5a_d9
	mcasp5_axr1/spi4_cs0/uart9_rtsn/uart3_txd/mlb_dat/vout2_d23/vin4a_d23/vin5a_d8
	xref_clk0/mcasp2_axr8/mcasp1_axr4/mcasp1_ahclkx/mcasp5_ahclkx/atl_clk0/vin6a_d0/hdq0/clkout2/timer13/gpio6_17
	xref_clk1/mcasp2_axr9/mcasp1_axr5/mcasp2_ahclkx/mcasp6_ahclkx/atl_clk1/vin6a_clk0/timer14/gpio6_18
	ref_clk2/mcasp2_axr10/mcasp1_axr5/mcasp3_ahclkx/mcasp7_ahclkx/atl_clk2/vout2_clk/vin4a_clk0/timer15/gpio6_19
	xref_clk3/mcasp2_axr11/mcasp1_axr7/mcasp4_ahclkx/mcasp8_ahclkx/atl_clk3/vout2_de/hdq0/vin4a_de0/clkout3/timer16/gpio6_20

B14		H_MCASP1_ACLKR
C14		H_MCASP1_ACLKX
J14		H_MCASP1_FSR
D14		H_MCASP1_FSX
G12		H_MCASP1_AXR0
F12		H_MCASP1_AXR1
G13		H_MCASP1_AXR2
J11		H_MCASP1_AXR3
E12		H_MCASP1_AXR4
F13		H_MCASP1_AXR5
C12		H_MCASP1_AXR6
D12		H_MCASP1_AXR7
B12		H_MCASP1_AXR8
A11		H_MCASP1_AXR9
B13		H_MCASP1_AXR10
A12		H_MCASP1_AXR11
E14		H_MCASP1_AXR12
A13		H_MCASP1_AXR13
G14		H_MCASP1_AXR14
F14		H_MCASP1_AXR15
E15		H_MCASP2_ACLKR
A19		H_MCASP2_ACLKX
A20		H_MCASP2_FSR
A18		H_MCASP2_FSX
B15		H_MCASP2_AXR0
A15		H_MCASP2_AXR1
C15		H_MCASP2_AXR2
A16		H_MCASP2_AXR3
D15		H_MCASP2_AXR4
B16		H_MCASP2_AXR5
B17		H_MCASP2_AXR6
A17		H_MCASP2_AXR7
B18		H_MCASP3_ACLKX
F15		H_MCASP3_AFSX
B19		H_MCASP3_AXR0
C17		H_MCASP3_AXR1
C18		H_MCASP4_ACLKX
A21		H_MCASP4_AFSX
G16		H_MCASP4_AXR0
D17		H_MCASP4_AXR1
AA3		H_MCASP5_ACLKX
AB9		H_MCASP5_AFSX
AB3		H_MCASP5_AXR0
AA4		H_MCASP5_AXR1
D18		H_XREF_CLK0
E17		H_XREF_CLK1
B26		H_XREF_CLK2
C23		H_XREF_CLK3

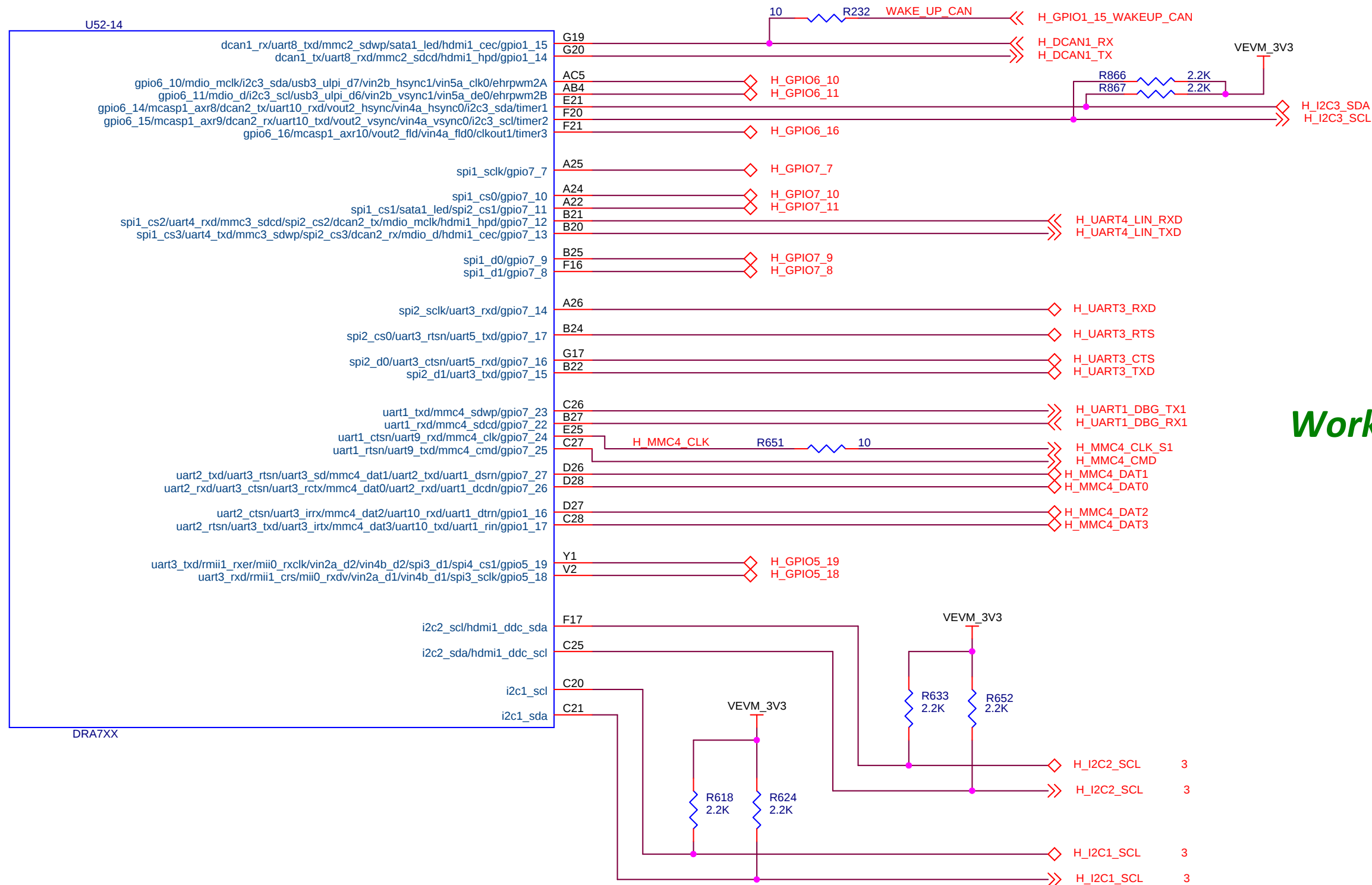
Work - In - Progress

DRA7XX

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu McASP			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 2 of		58

TI CONFIDENTIAL - NDA RESTRICTIONS



Work - In - Progress

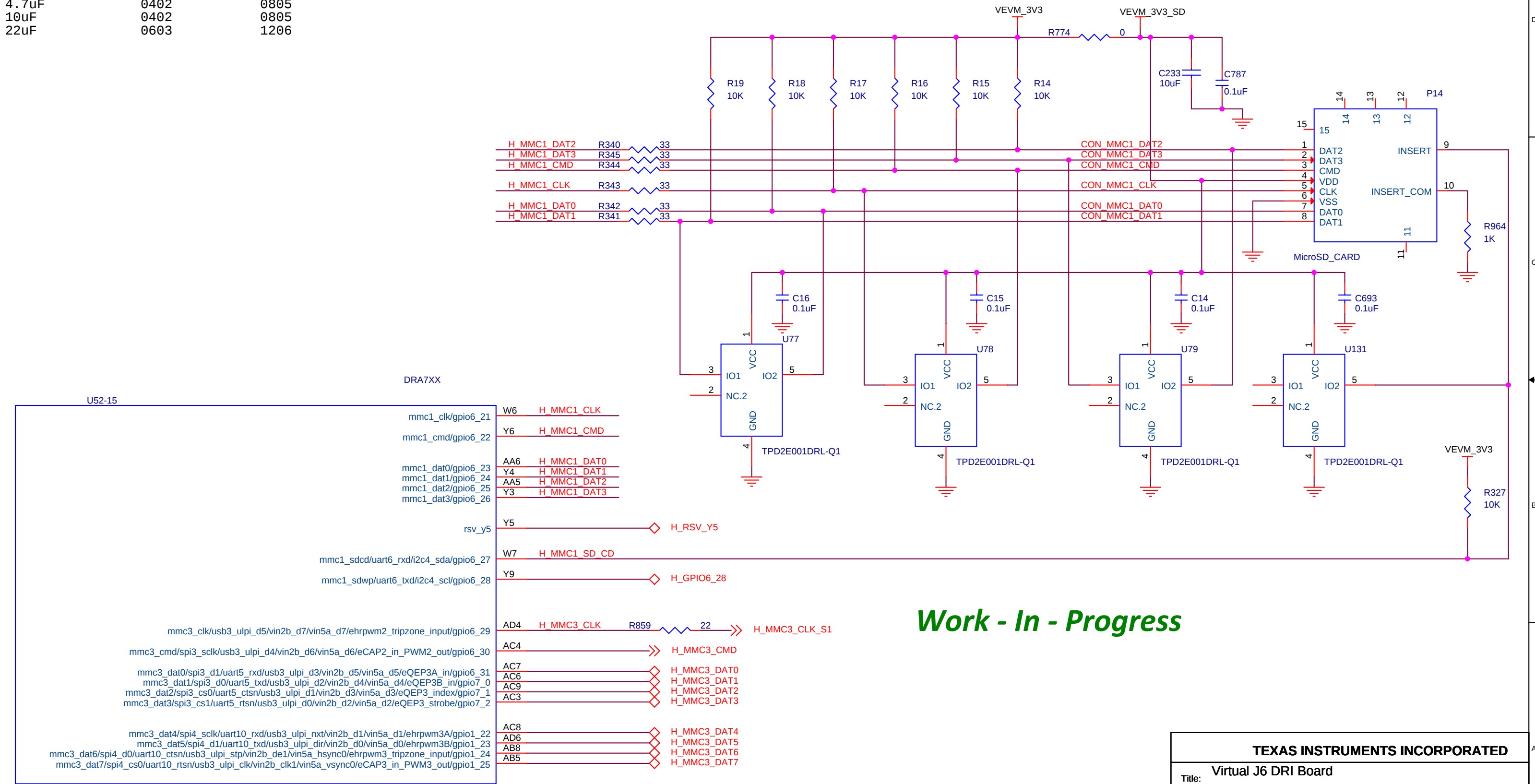
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Serial I/O			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 3 of		58

CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

TI CONFIDENTIAL - NDA RESTRICTIONS

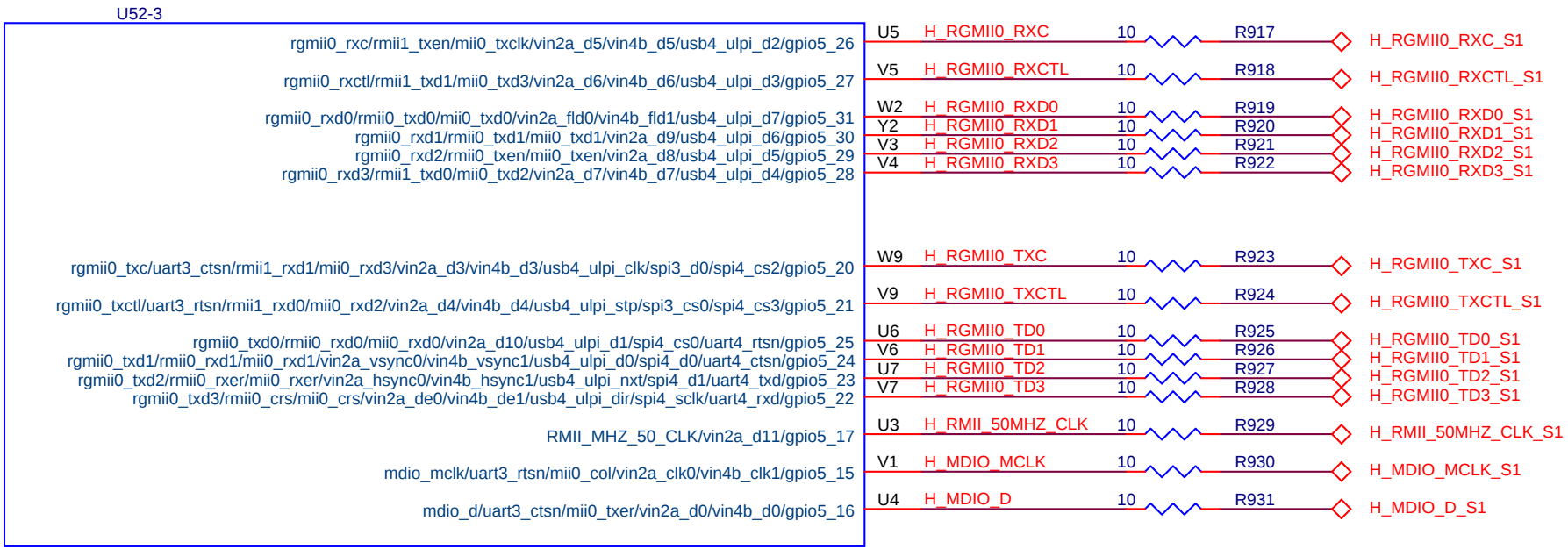
Auto Cap Sizes Updated



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu SD/MMC			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 4 of		58

TI CONFIDENTIAL - NDA RESTRICTIONS



DRA7XX

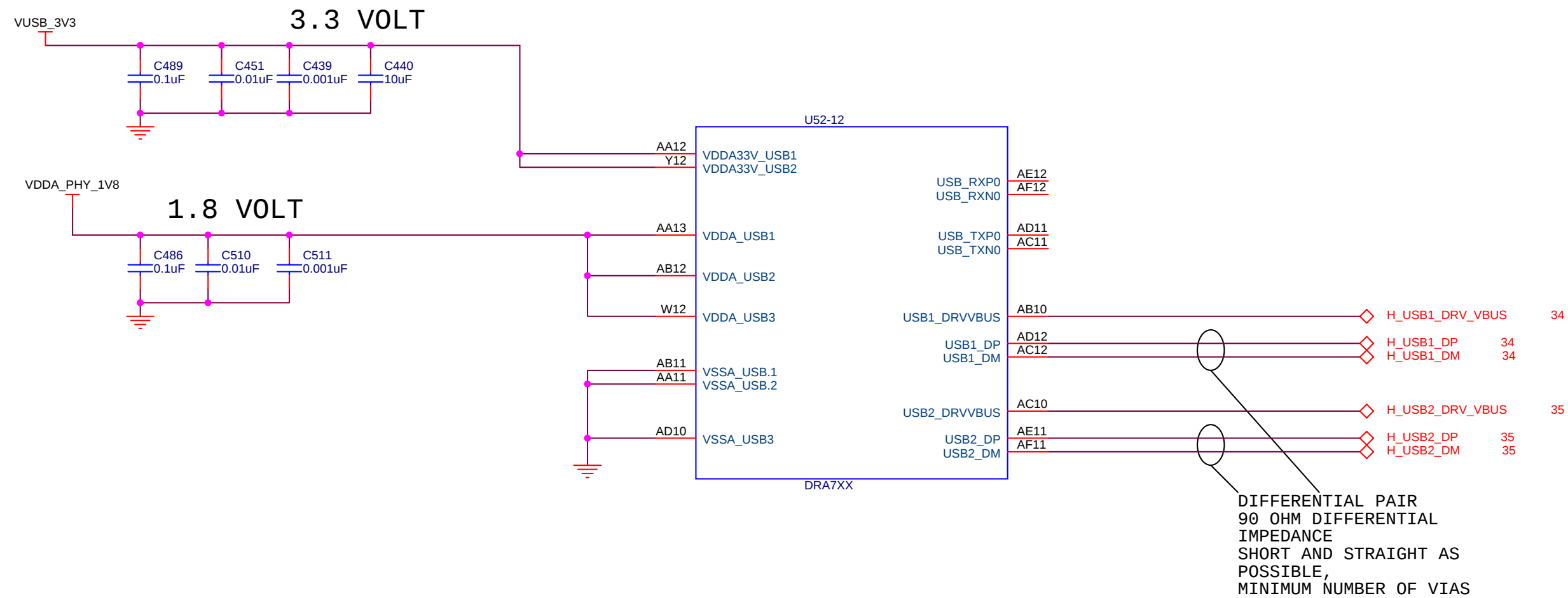
Work - In - Progress

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Ethernet			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 5 of 58		

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated



Work - In - Progress

CAPACITANCE	Commerical Size/X5R	Automotive Size/X7R
Vaule		
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu USB			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 6 of		58



TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu GPMC			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 7 of		58

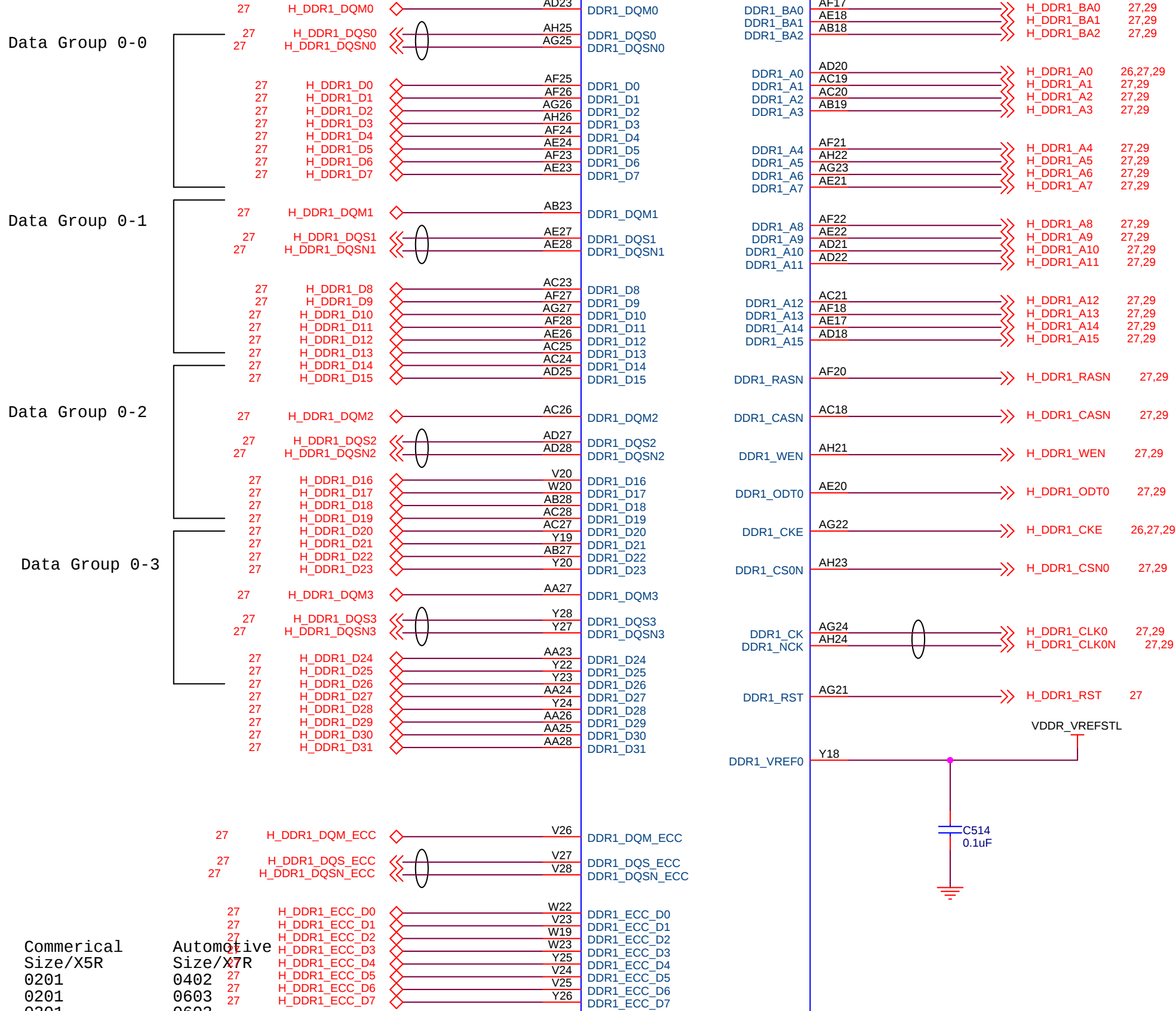
EACH DATA GROUP IS MATCHED WITHIN THE GROUP

USE 4X SPACING TRACE-TO-TRACE;
"FLIGHT-TIME MATCHING" PREFERRED
OVER "LENGTH MATCHING."

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated

6 places



Work - In - Progress

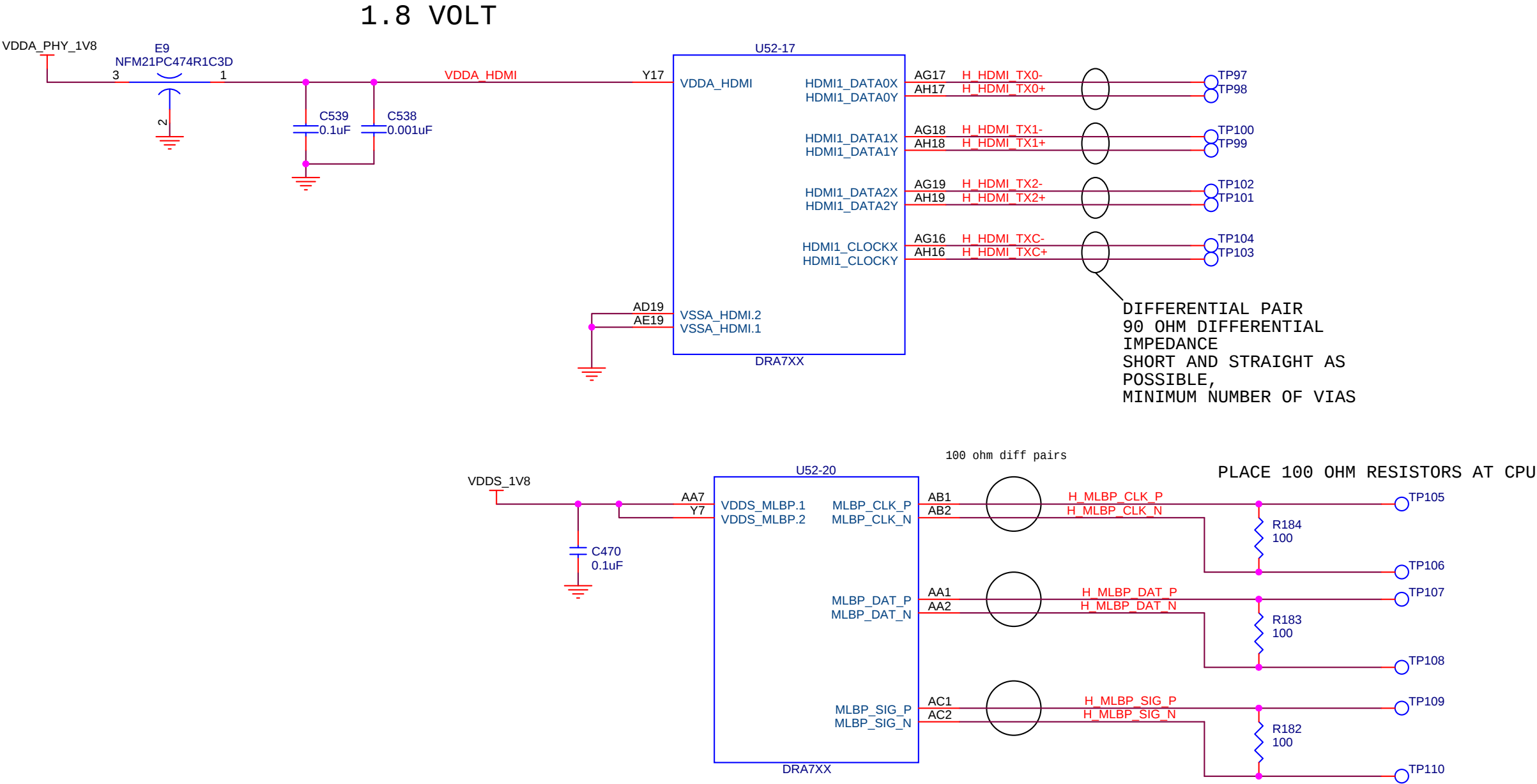
CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu EMIF1			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 8 of		58

Auto Cap Sizes Updated

Work - In - Progress

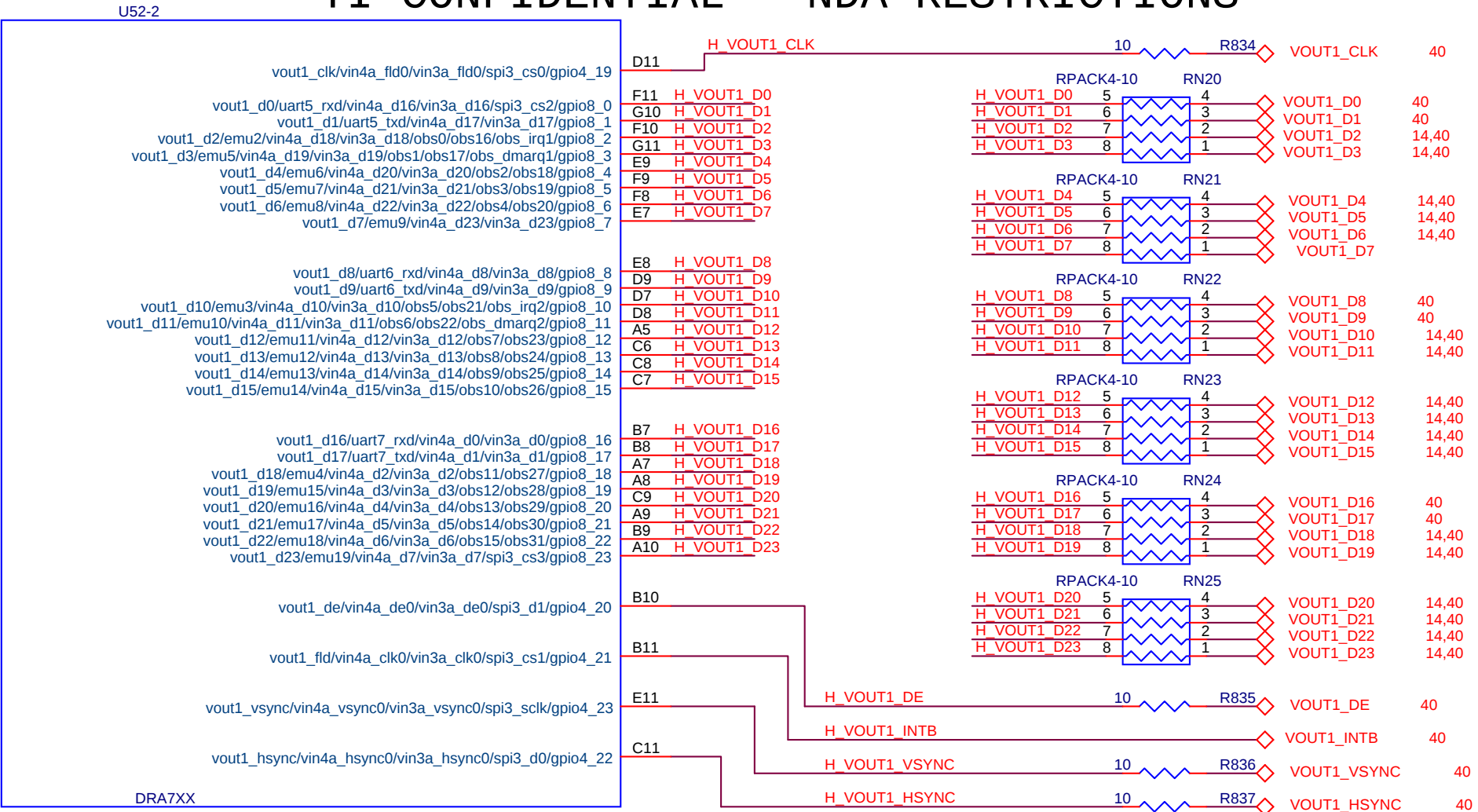


CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu HDMI MLB			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 10 of		58

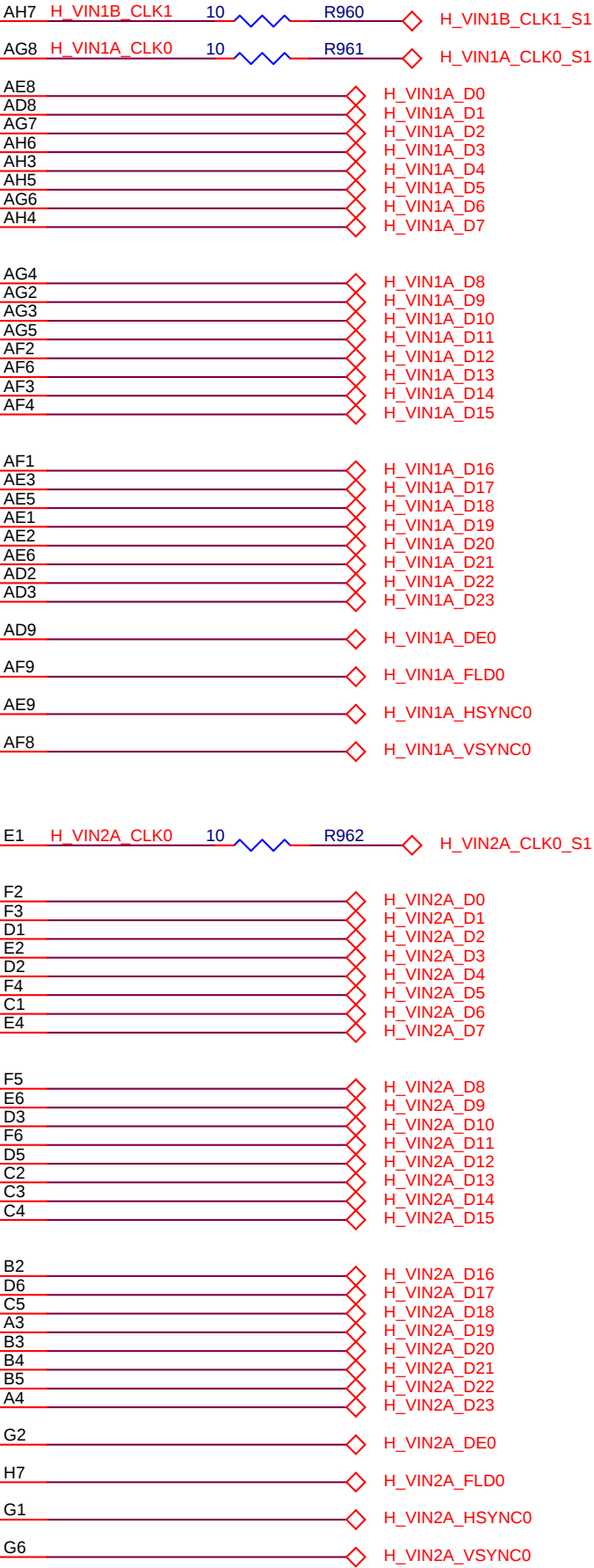
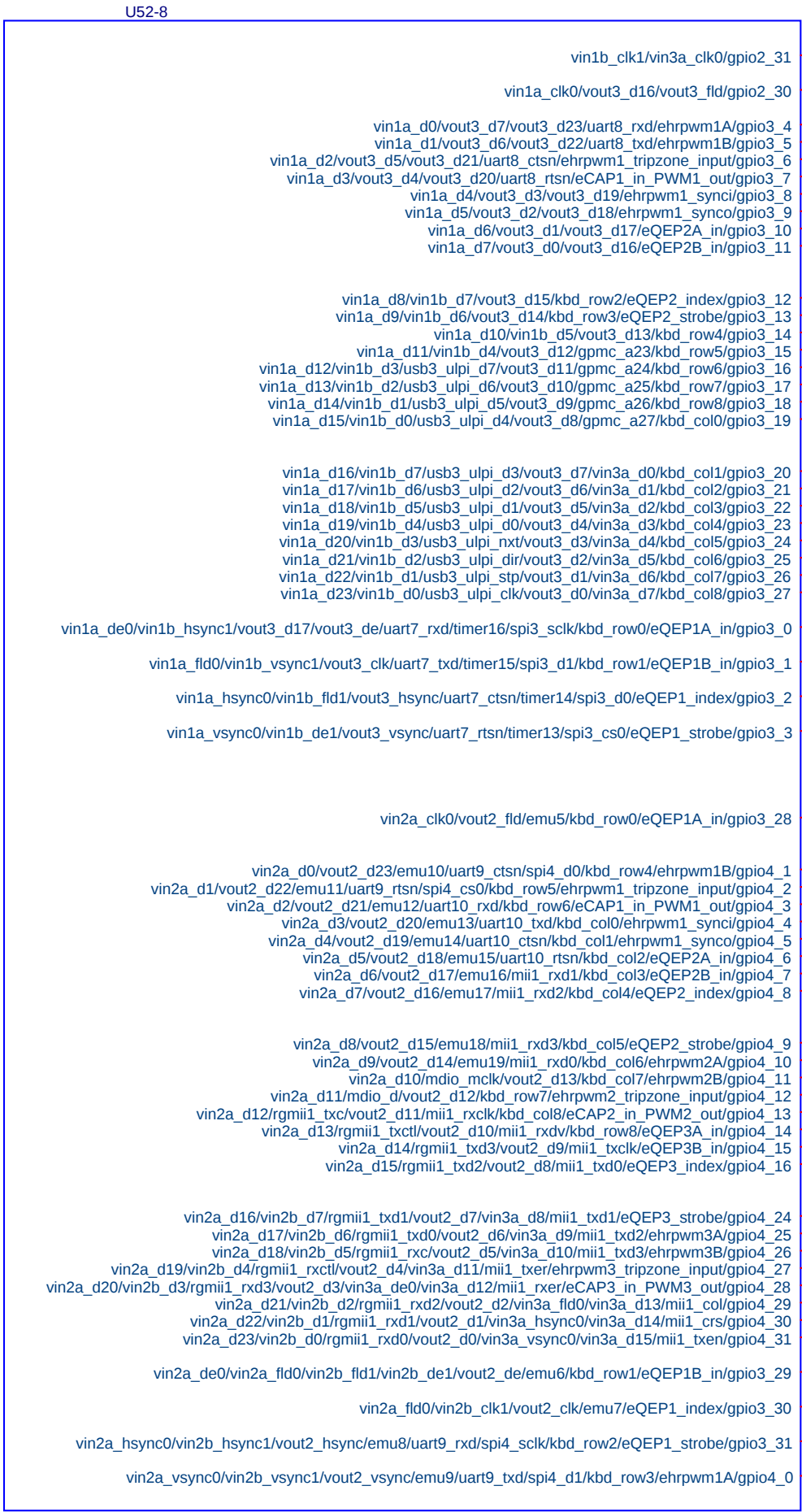
TI CONFIDENTIAL - NDA RESTRICTIONS



Work - In - Progress

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu VOUT1/LCD Port			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 11 of		58



Work - In - Progress

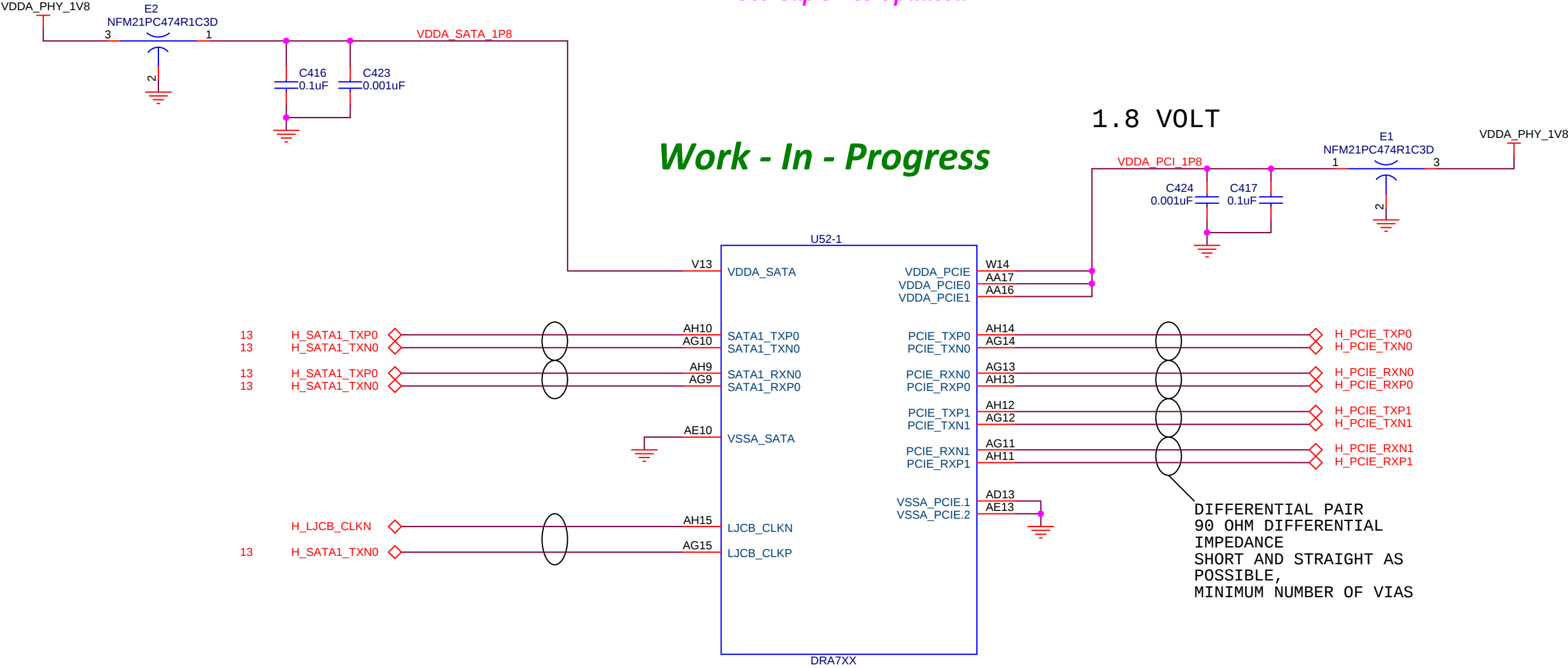
TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Video Input Ports			
Size:B	DWG NO	tbđ	Revision: A
Date: Tuesday, December 10, 2013		Sheet 12 of	58

Auto Cap Sizes Updated

1.8 VOLT

1.8 VOLT

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

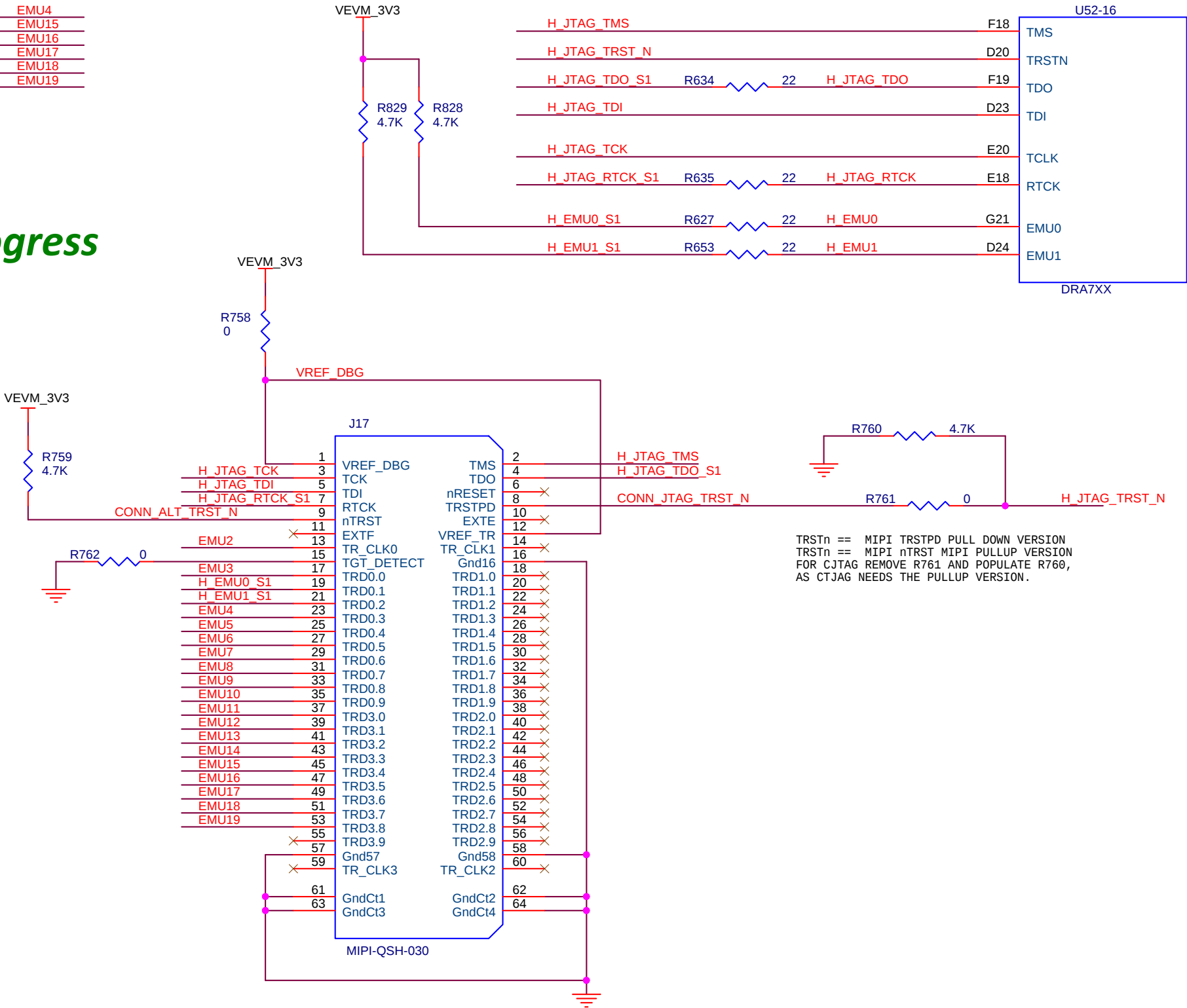
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu SATA PCIe			
Size:B	DWG NO	tbd	Revision: A
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11,40	VOUT1_D2	EMU2	11,40	VOUT1_D10	EMU3	11,40	VOUT1_D18	EMU4
11,40	VOUT1_D3	EMU5	11,40	VOUT1_D11	EMU10	11,40	VOUT1_D19	EMU15
11,40	VOUT1_D4	EMU6	11,40	VOUT1_D12	EMU11	11,40	VOUT1_D20	EMU16
11,40	VOUT1_D5	EMU7	11,40	VOUT1_D13	EMU12	11,40	VOUT1_D21	EMU17
11,40	VOUT1_D6	EMU8	11,40	VOUT1_D14	EMU13	11,40	VOUT1_D22	EMU18
40	VOUT_D7	EMU9	11,40	VOUT1_D15	EMU14	11,40	VOUT1_D23	EMU19

Work - In - Progress

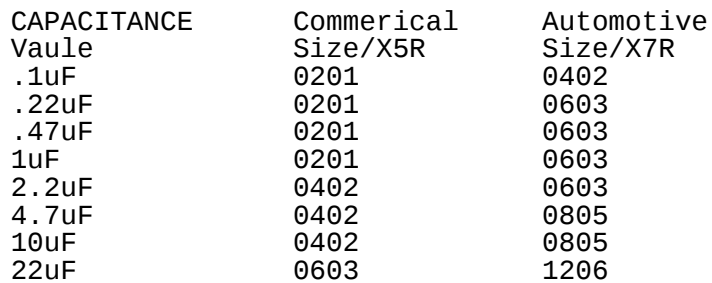


Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu JTAG Trace			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 14 of		58

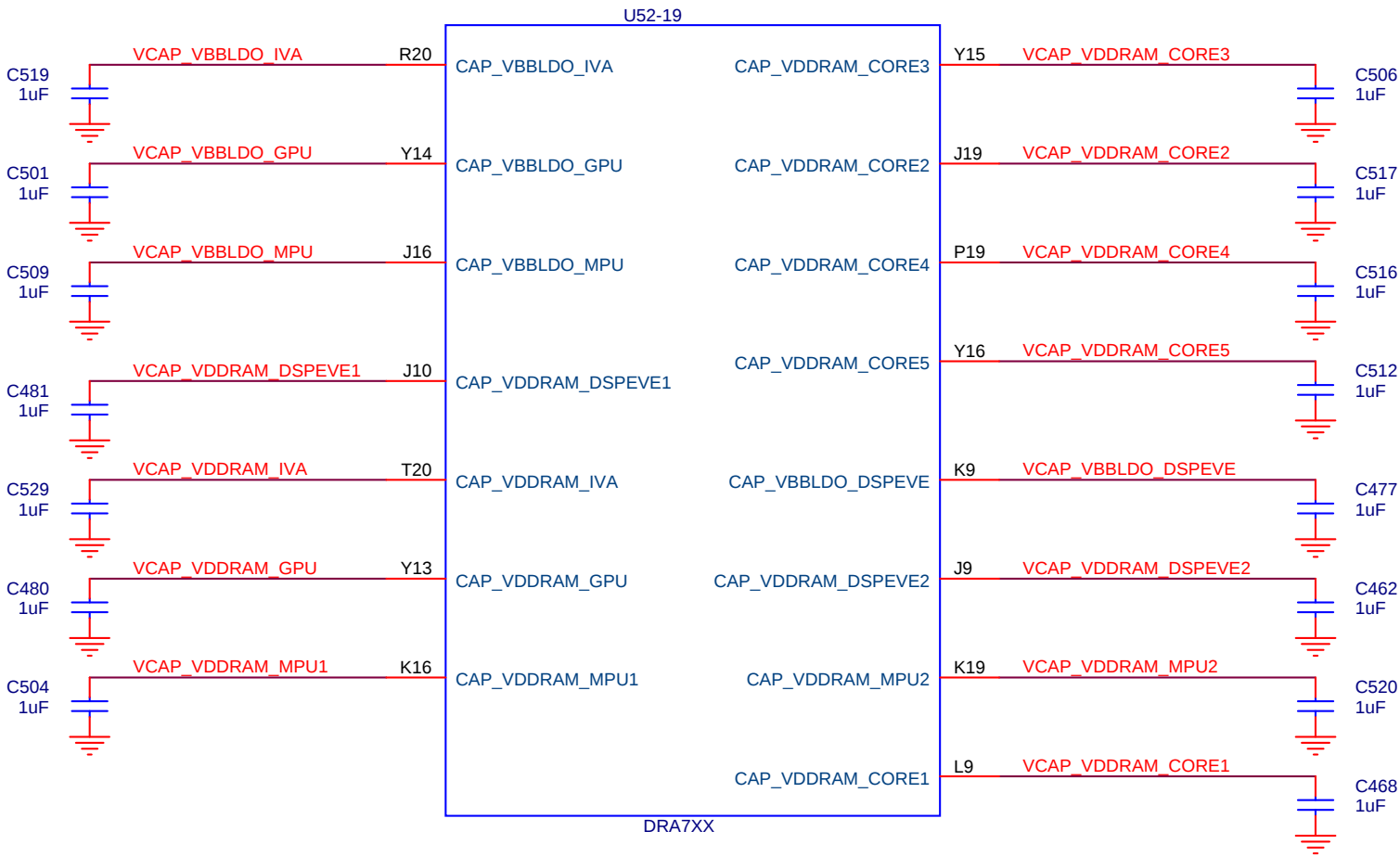
Auto Cap Sizes Updated

Note: WAKEUP[3:0], including the GP1[x] functions, are input-only.



TEXAS INSTRUMENTS INCORPORATED		
Title: Virtual J6 DRI Board		
Page Contents: Vayu Clocks		
Size:B	DWG NO tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 15 of	58

Auto Cap Sizes Updated



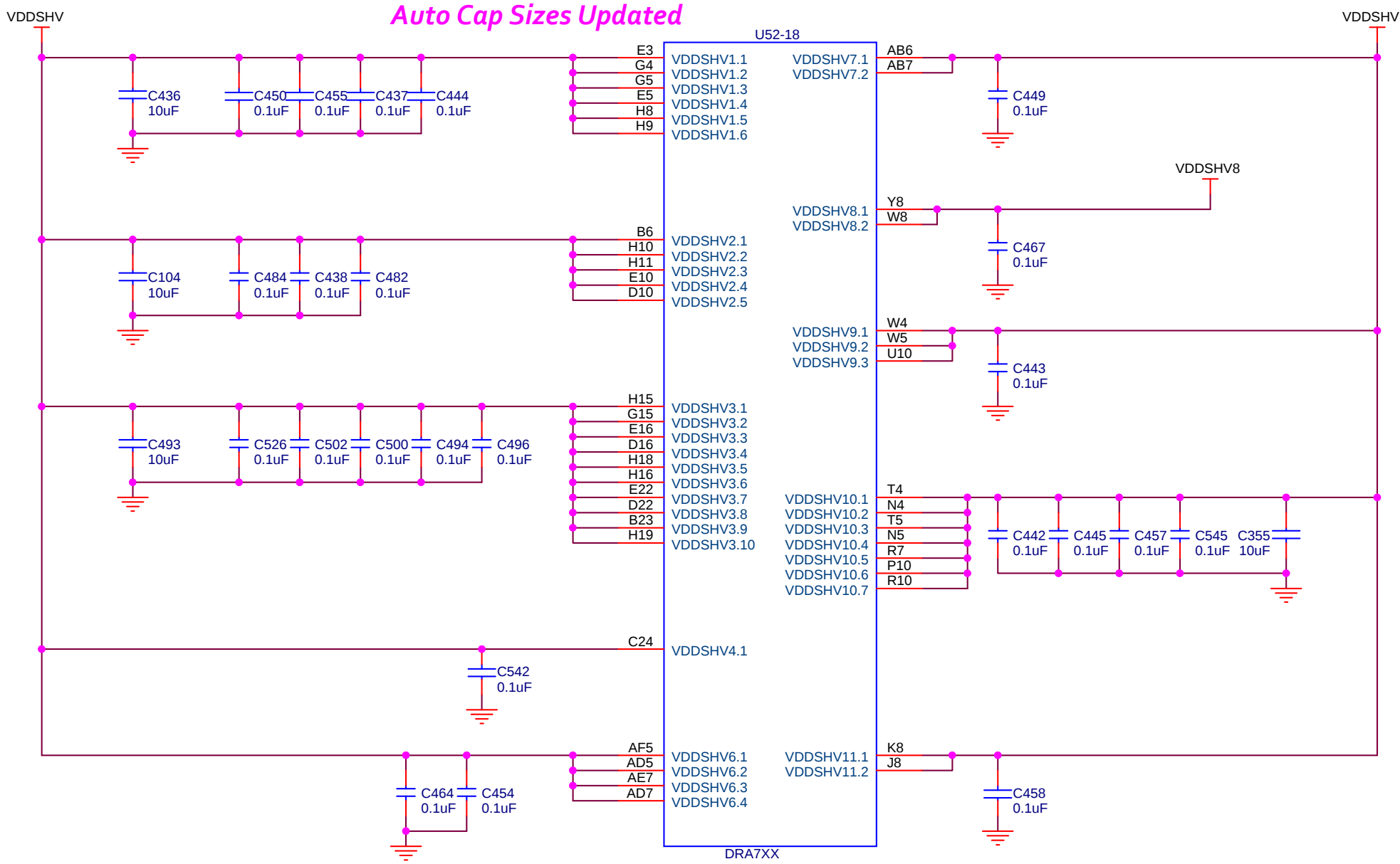
Work - In - Progress

CAPACITANCE	Commerical	Automotive
Value	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Internal LDOs			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 16 of		58

TI CONFIDENTIAL - NDA RESTRICTIONS



Work - In - Progress

CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

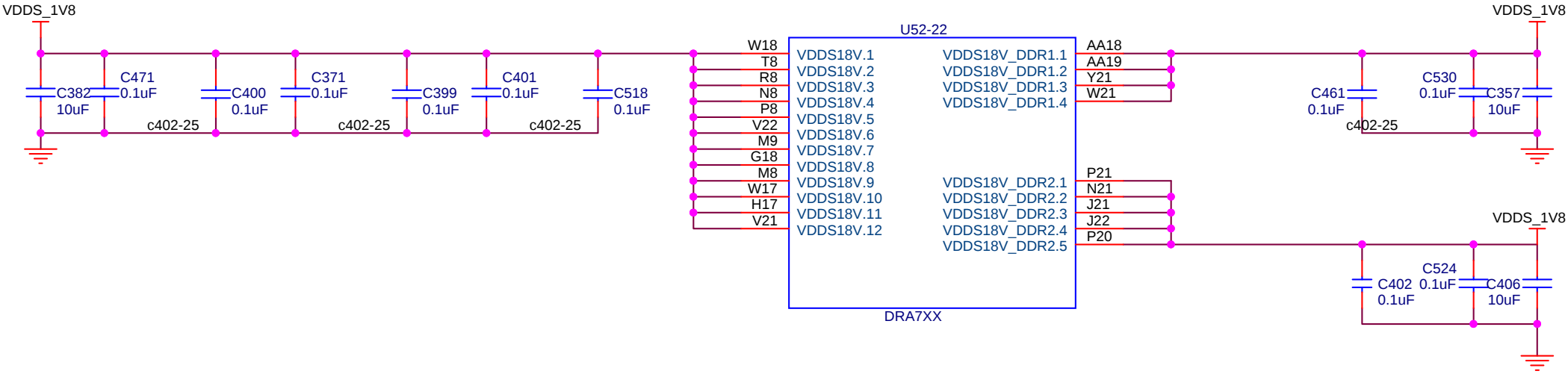
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu IO Power			
Size:B	DWG NO	tbd	Revision: A
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TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

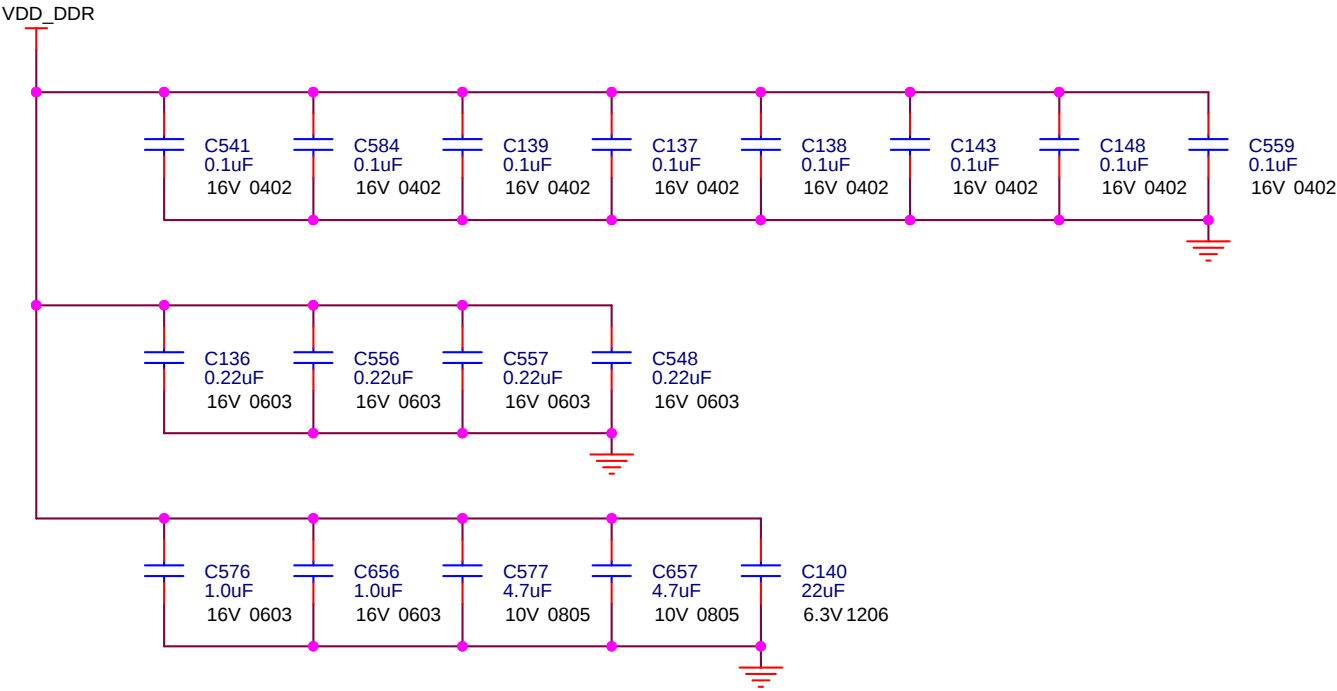
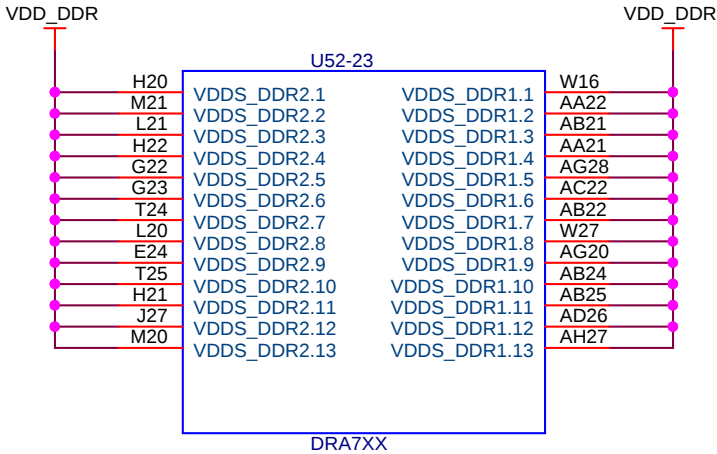
TEXAS INSTRUMENTS INCORPORATED		
Title: Virtual J6 DRI Board		
Page Contents: Vayu 1V8 Digital Power		
Size:B	DWG NO tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 18 of	58

Preliminary Information - Subject to change

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

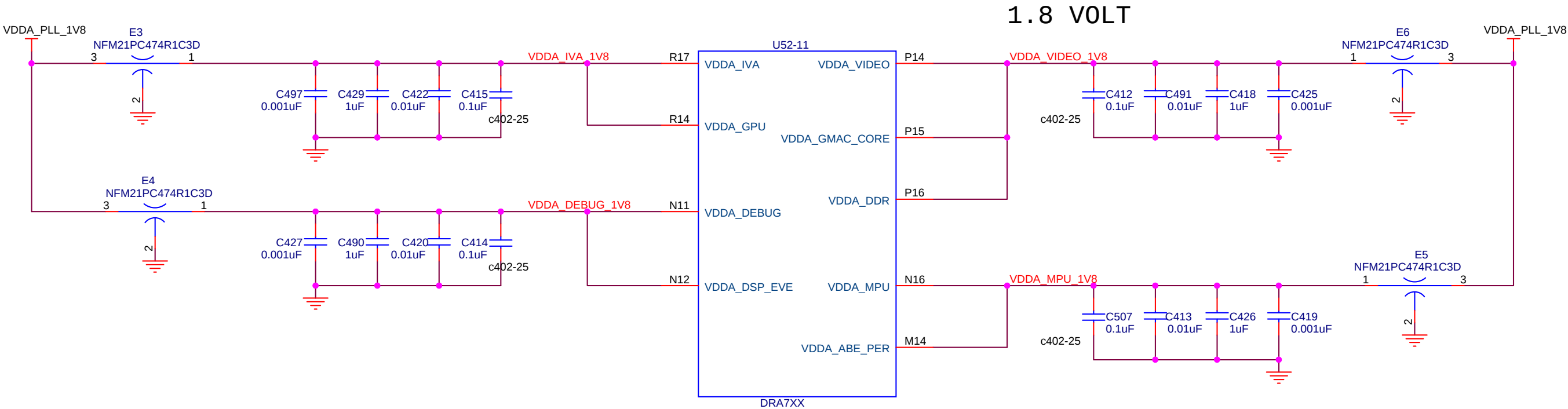
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR Power			
Size:B	DWG NO	tbd	Revision: B
Date: Tuesday, December 10, 2013	Sheet 19 of		58

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated
Verified EMI filters E3-E6 are +125C rated & 0805

Work - In - Progress



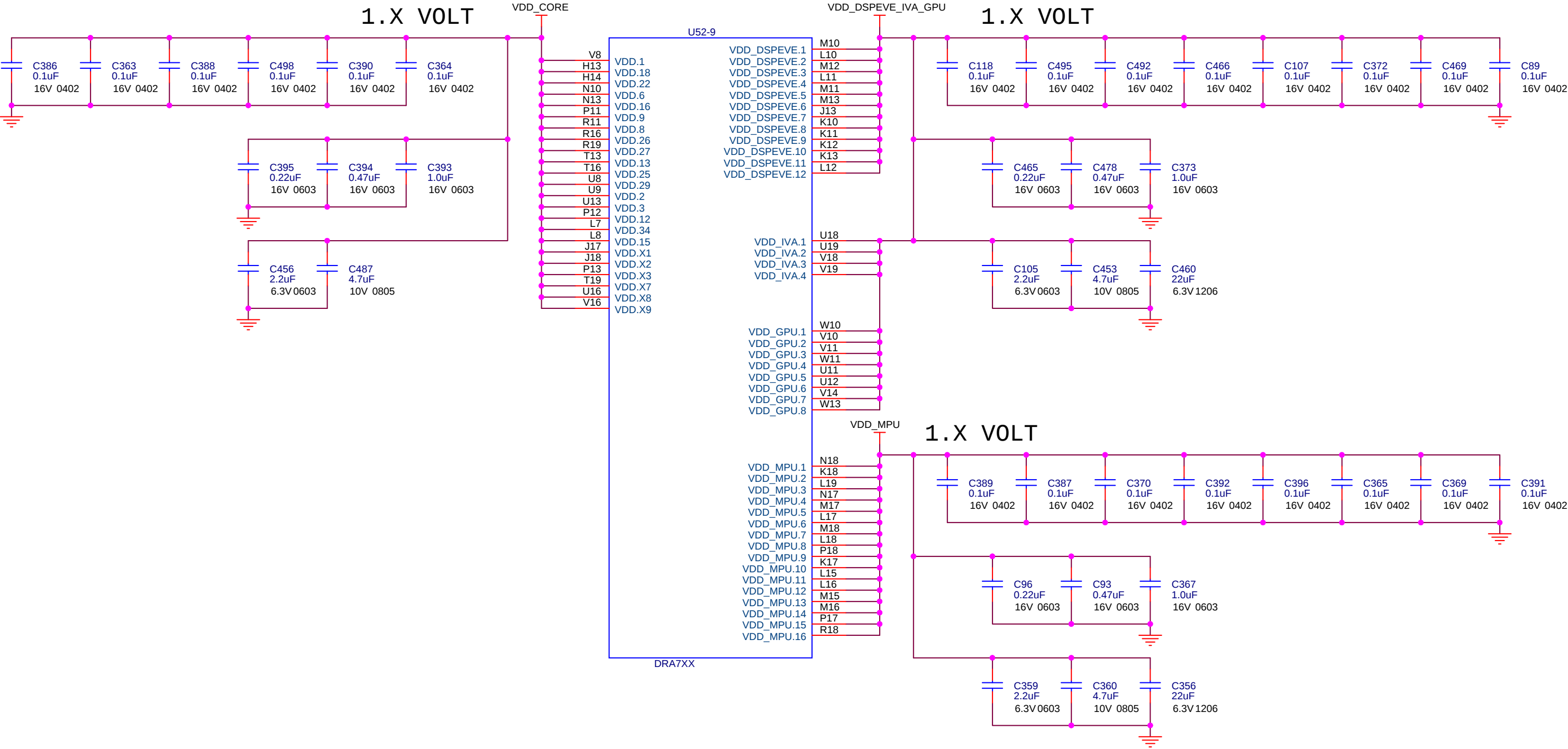
CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu 1V8 Analog Power			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 20 of		58

Auto Cap Sizes Updated

Work - In - Progress

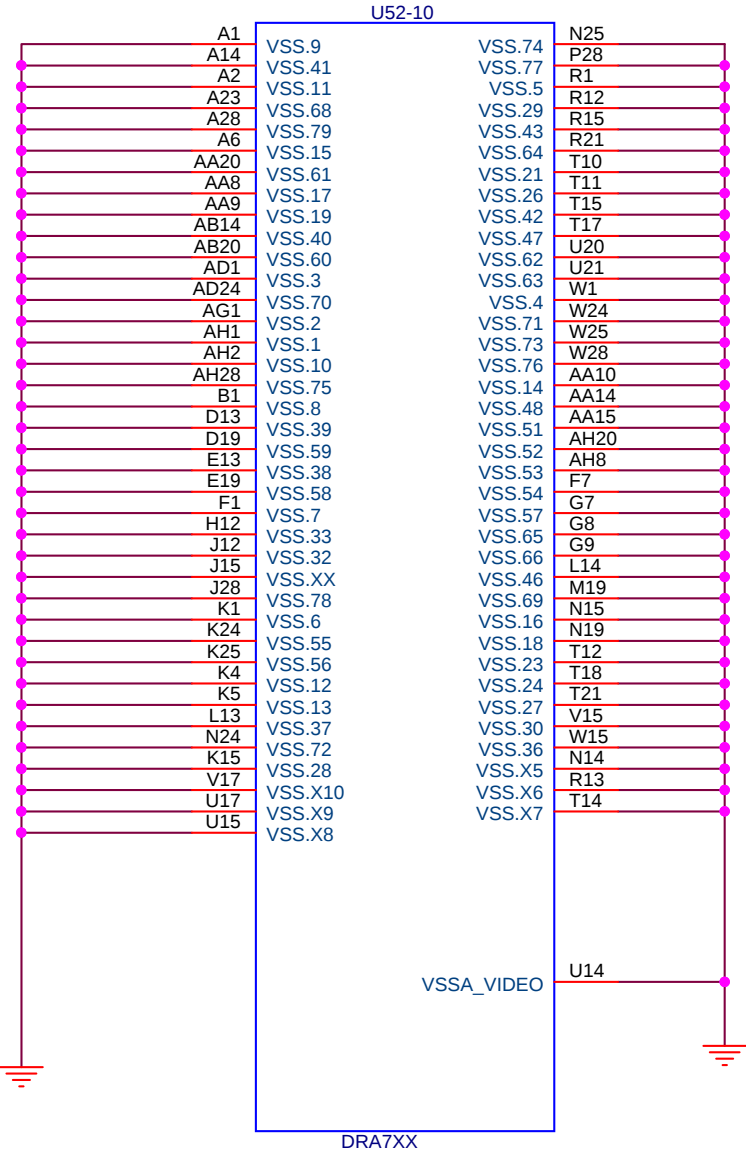


CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu AVS Power			
Size:B	DWG NO	tbd	Revision: B
Date: Tuesday, December 10, 2013	Sheet 21 of		58

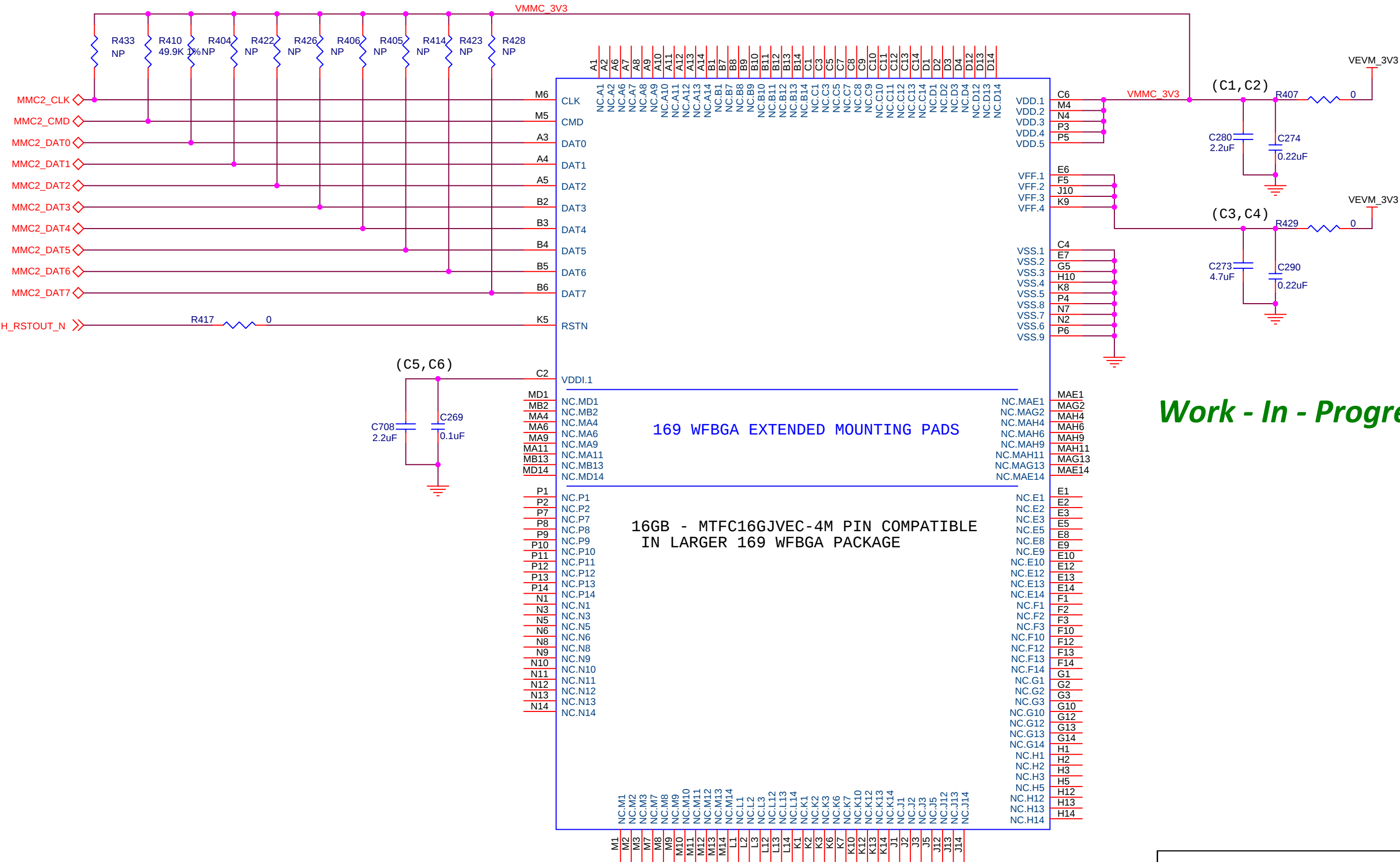
TI CONFIDENTIAL - NDA
RESTRICTIONS



Work - In - Progress

Preliminary Information - Subject to change

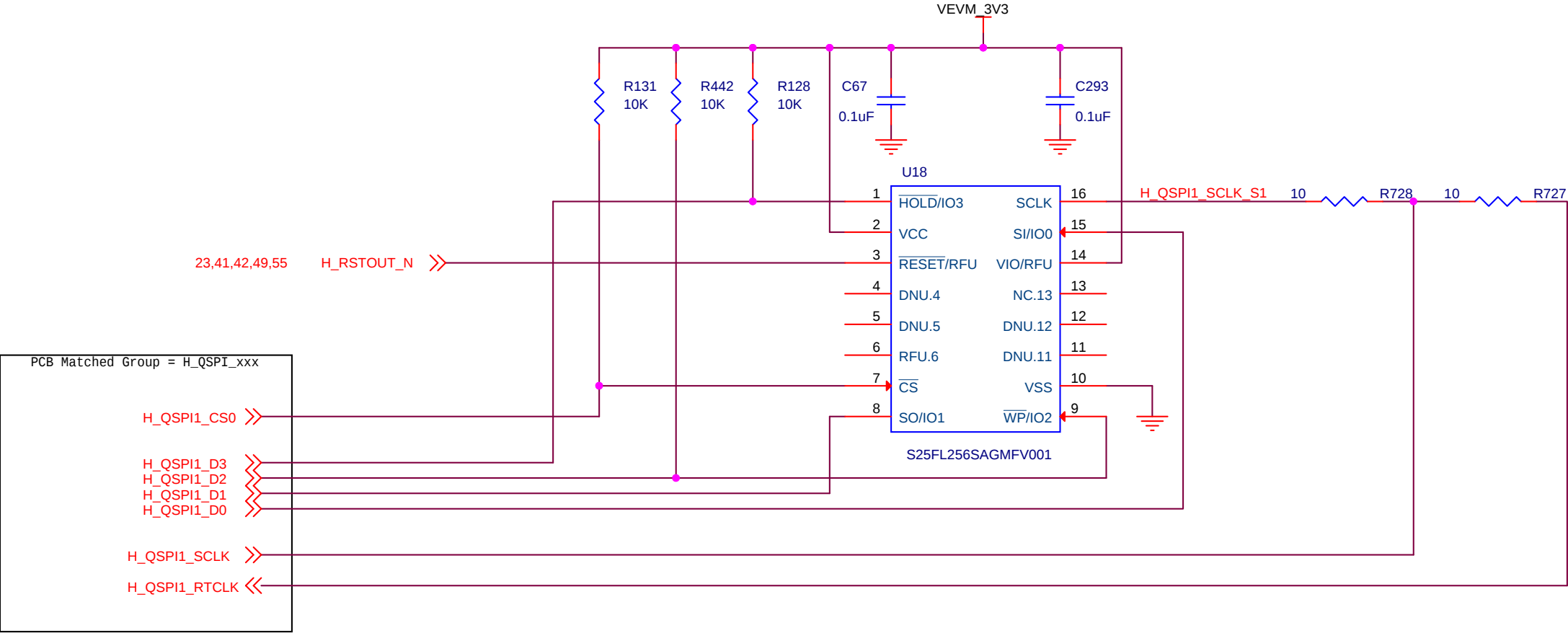
TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Ground			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 22 of		58



Work - In - Progress

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: eMMC Flash Memory			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 23 of 58		

Work - In - Progress



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: QSPI Flash Memory			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 24 of		58

SoC Signaling Modes on specific balls

i2c2_sda
i2c2_scl

hdmi1_ddc_scl
hdmi1_ddc_sda

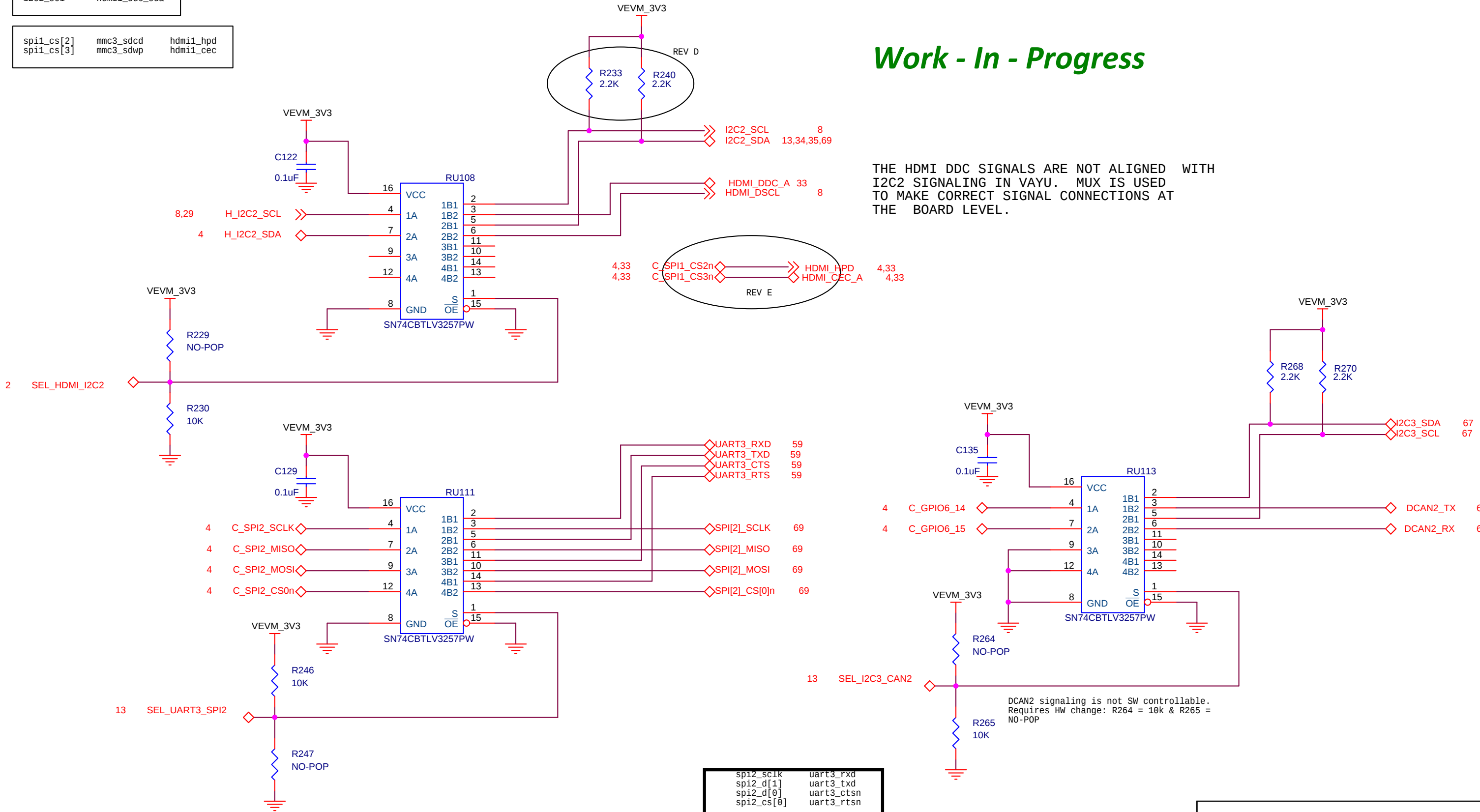
spi1_cs[2]
spi1_cs[3]

mmc3_sdcd
mmc3_sdwp

hdmi1_hpd
hdmi1_cec

Work - In - Progress

THE HDMI DDC SIGNALS ARE NOT ALIGNED WITH I2C2 SIGNALING IN VAYU. MUX IS USED TO MAKE CORRECT SIGNAL CONNECTIONS AT THE BOARD LEVEL.



spi2_sclk
spi2_d[1]
spi2_d[0]
spi2_cs[0]

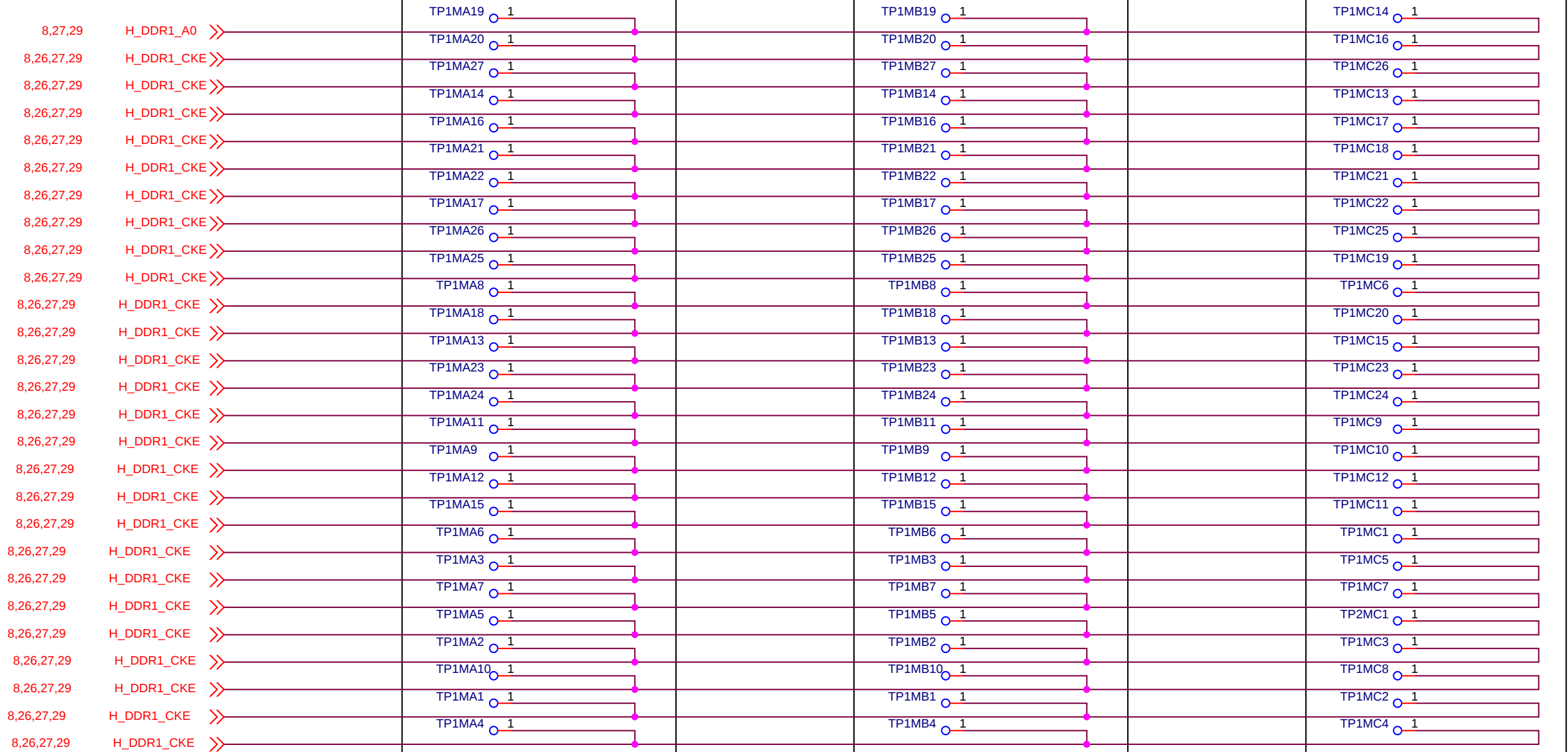
uart3_rxd
uart3_txd
uart3_ctsn
uart3_rtsn

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SERIAL I/O MUX			
Size: B	DWG NO	516582-0001	Revision: E
Date: Tuesday, December 10, 2013	Sheet 25 of		58

Work - In - Progress

TI CONFIDENTIAL - NDA RESTRICTIONS



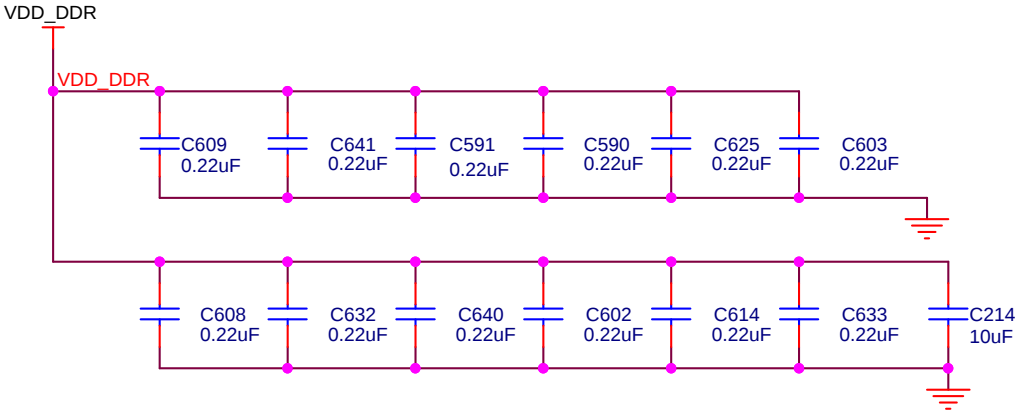
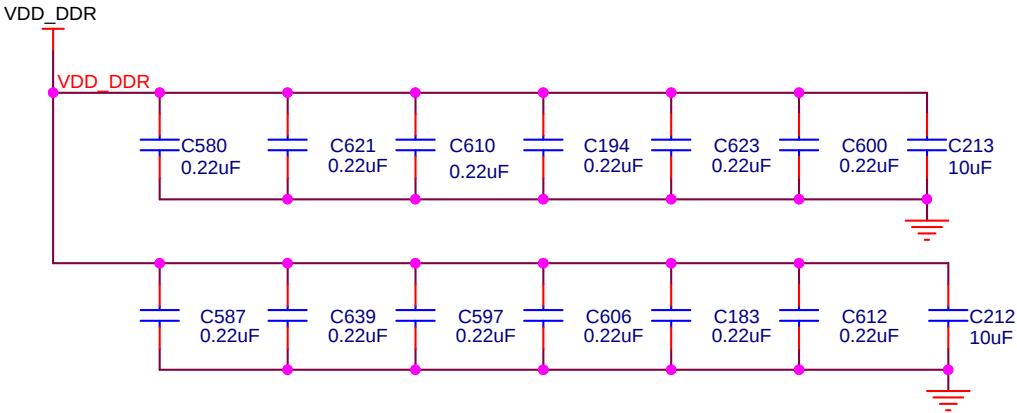
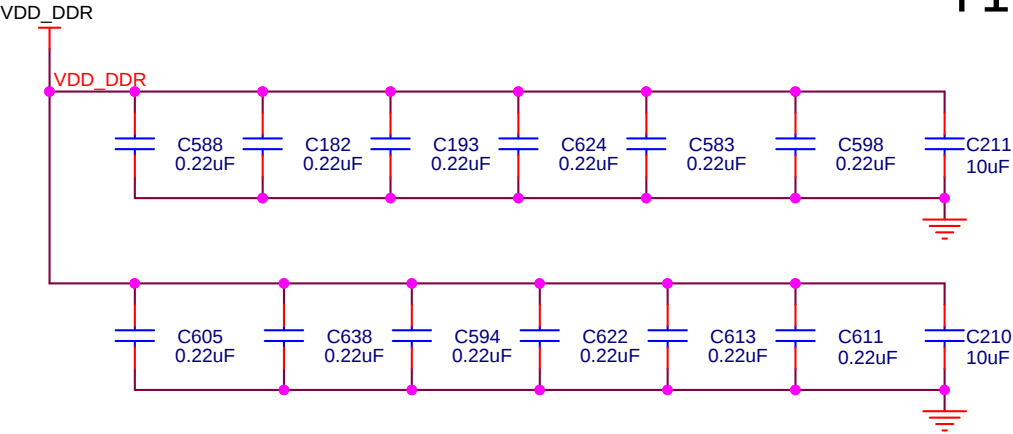
TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR3 EMIF1 Test Points			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 26 of		58



TEXAS INSTRUMENTS INCORPORATED		
Title: Virtual J6 DRI Board		
Page Contents: Vayu DDR3 EMIF1 Bank1		
Size:B	DWG NO tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 27 of	58

Auto Cap Sizes Updated

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

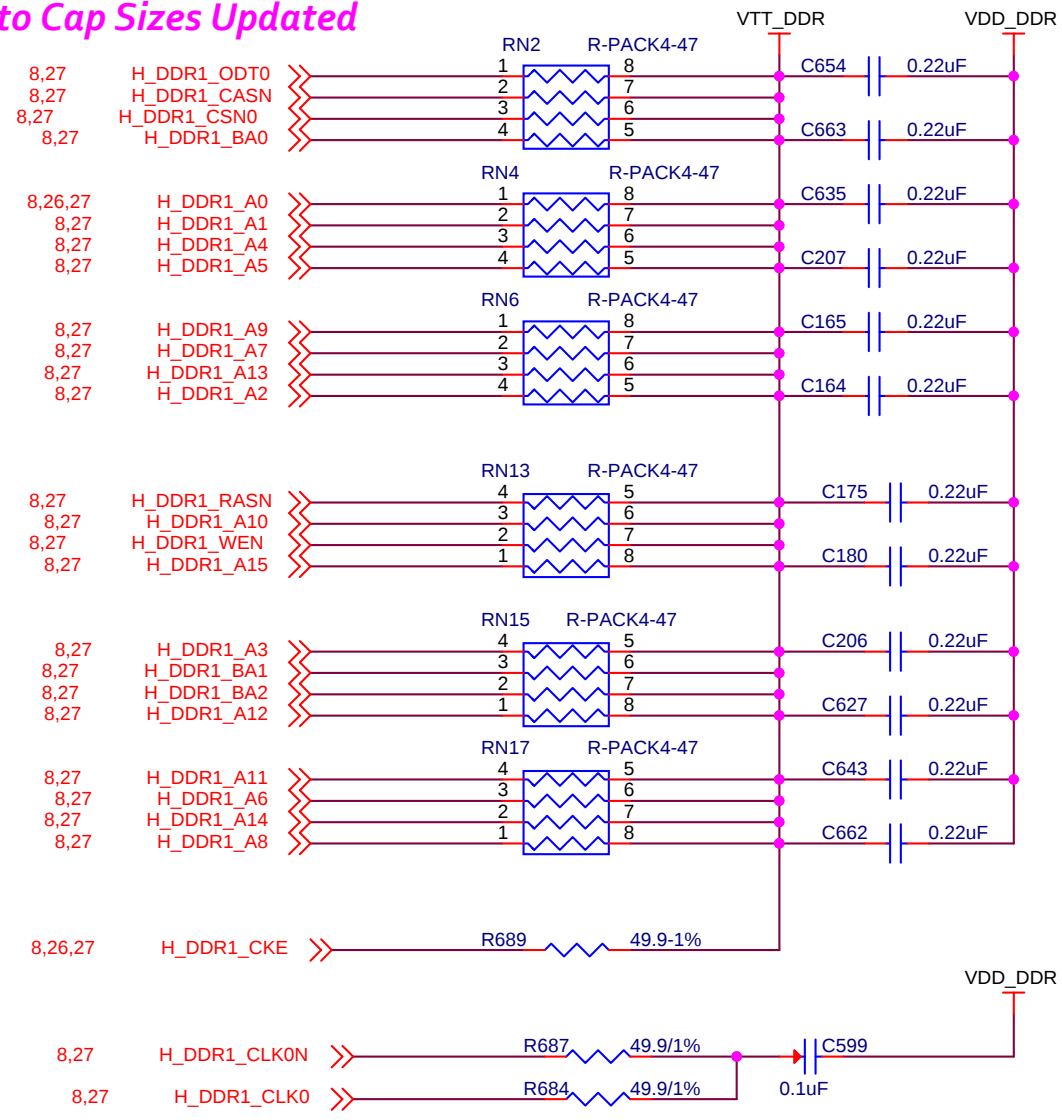
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu Bank1 Caps			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 28 of		58

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated

Work - In - Progress

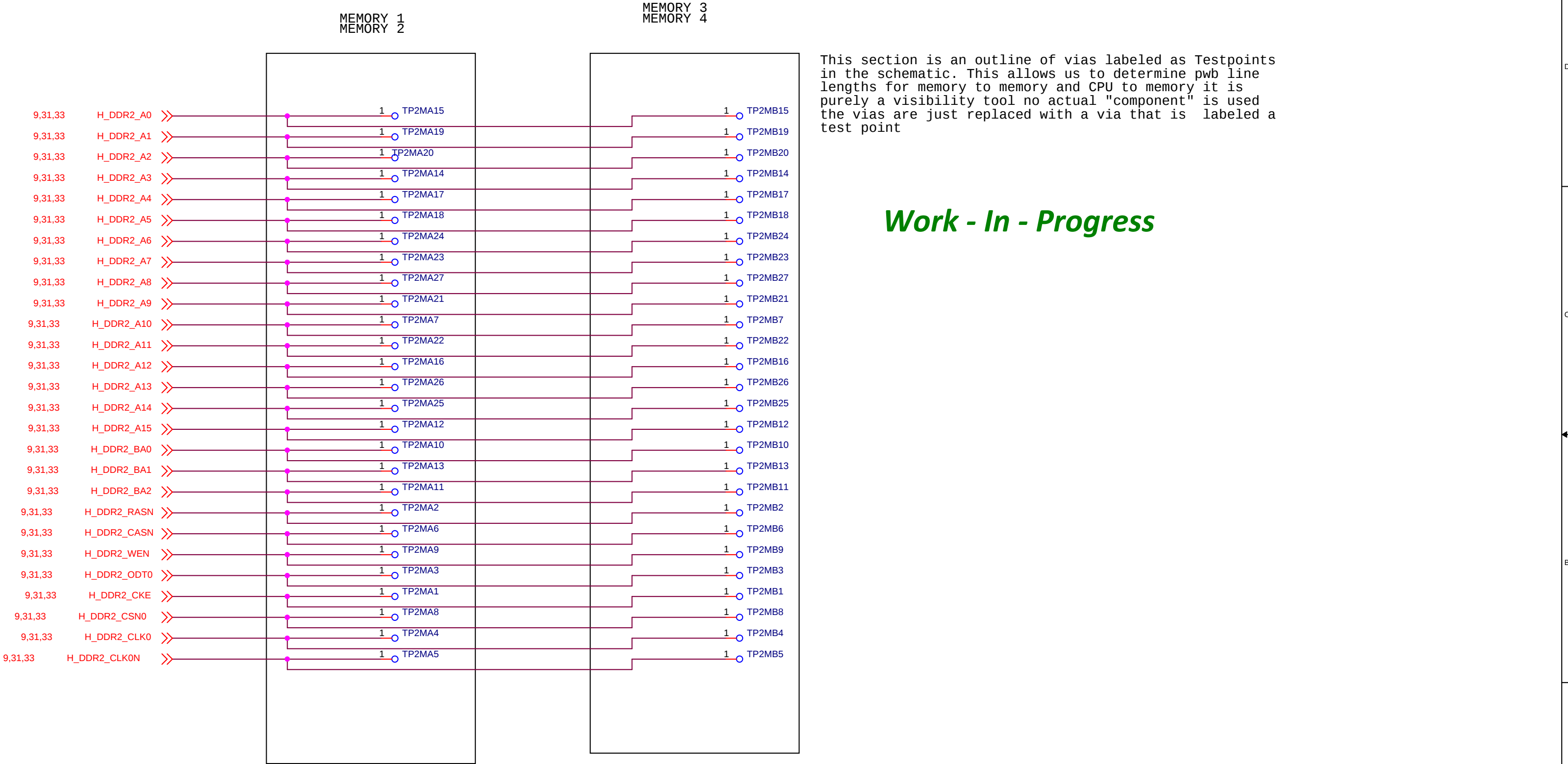


CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR3 EMIF1 Termination			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013			Sheet 29 of 58

TI CONFIDENTIAL - NDA RESTRICTIONS



This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point

Work - In - Progress

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR3 EMIF2 Test Points			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 30 of		58

Auto Cap Sizes Updated

TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

H_DDR2_A0 K3
H_DDR2_A1 L7
H_DDR2_A2 L3
H_DDR2_A3 K2
H_DDR2_A4 L8
H_DDR2_A5 L2
H_DDR2_A6 M8
H_DDR2_A7 M2
H_DDR2_A8 N8
H_DDR2_A9 M3
H_DDR2_A10 H7
H_DDR2_A11 M7
H_DDR2_A12 K7
H_DDR2_A13 N3
H_DDR2_A14 N7
H_DDR2_A15 J7

B3 H_DDR2_D7
C7 H_DDR2_D4
C2 H_DDR2_D6
C8 H_DDR2_D2
E3 H_DDR2_D5
E8 H_DDR2_D3
D2 H_DDR2_D1
E7 H_DDR2_D0
B7 H_DDR2_DQM0
A7 H_DDR2_DQS0
C3 H_DDR2_DQSN0
D3 H_DDR2_DQSN0

DM/TDQS
TDQS
DQS
DQS

NC.1
NC.2
NC.3
NC.4
NC.5

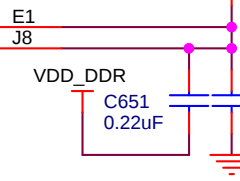
H_DDR2_BA0 J2
H_DDR2_BA1 K8
H_DDR2_BA2 J3

H_DDR2_RASn F3
H_DDR2_CASn G3
H_DDR2_WEn H3
H_DDR2_ODT0 G1
H_DDR2_CKE G9
H_DDR2_CSN0 H2

H_DDR2_CLK0 F7
H_DDR2_CLK0NG7

H_DDR2_RST N2

VREFDQ
VREFCA



H_DDR2_A0 K3
H_DDR2_A1 L7
H_DDR2_A2 L3
H_DDR2_A3 K2
H_DDR2_A4 L8
H_DDR2_A5 L2
H_DDR2_A6 M8
H_DDR2_A7 M2
H_DDR2_A8 N8
H_DDR2_A9 M3
H_DDR2_A10 H7
H_DDR2_A11 M7
H_DDR2_A12 K7
H_DDR2_A13 N3
H_DDR2_A14 N7
H_DDR2_A15 J7

B3 H_DDR2_D13
C7 H_DDR2_D11
C2 H_DDR2_D14
C8 H_DDR2_D12
E3 H_DDR2_D8
E8 H_DDR2_D10
D2 H_DDR2_D15
E7 H_DDR2_D9
B7 H_DDR2_DQM1
A7 H_DDR2_DQS1
C3 H_DDR2_DQSN1
D3 H_DDR2_DQSN1

DM/TDQS
TDQS
DQS
DQS

NC.1
NC.2
NC.3
NC.4
NC.5

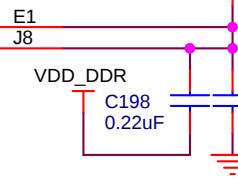
H_DDR2_BA0 J2
H_DDR2_BA1 K8
H_DDR2_BA2 J3

H_DDR2_RASn F3
H_DDR2_CASn G3
H_DDR2_WEn H3
H_DDR2_ODT0 G1
H_DDR2_CKE G9
H_DDR2_CSN0 H2

H_DDR2_CLK0 F7
H_DDR2_CLK0NG7

H_DDR2_RST N2

VREFDQ
VREFCA



H_DDR2_A0 K3
H_DDR2_A1 L7
H_DDR2_A2 L3
H_DDR2_A3 K2
H_DDR2_A4 L8
H_DDR2_A5 L2
H_DDR2_A6 M8
H_DDR2_A7 M2
H_DDR2_A8 N8
H_DDR2_A9 M3
H_DDR2_A10 H7
H_DDR2_A11 M7
H_DDR2_A12 K7
H_DDR2_A13 N3
H_DDR2_A14 N7
H_DDR2_A15 J7

B3 H_DDR2_D18
C7 H_DDR2_D16
C2 H_DDR2_D17
C8 H_DDR2_D19
E3 H_DDR2_D22
E8 H_DDR2_D20
D2 H_DDR2_D23
E7 H_DDR2_D21
B7 H_DDR2_DQM2
A7 H_DDR2_DQS2
C3 H_DDR2_DQSN2
D3 H_DDR2_DQSN2

DM/TDQS
TDQS
DQS
DQS

NC.1
NC.2
NC.3
NC.4
NC.5

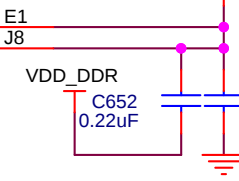
H_DDR2_BA0 J2
H_DDR2_BA1 K8
H_DDR2_BA2 J3

H_DDR2_RASn F3
H_DDR2_CASn G3
H_DDR2_WEn H3
H_DDR2_ODT0 G1
H_DDR2_CKE G9
H_DDR2_CSN0 H2

H_DDR2_CLK0 F7
H_DDR2_CLK0NG7

H_DDR2_RST N2

VREFDQ
VREFCA



H_DDR2_A0 K3
H_DDR2_A1 L7
H_DDR2_A2 L3
H_DDR2_A3 K2
H_DDR2_A4 L8
H_DDR2_A5 L2
H_DDR2_A6 M8
H_DDR2_A7 M2
H_DDR2_A8 N8
H_DDR2_A9 M3
H_DDR2_A10 H7
H_DDR2_A11 M7
H_DDR2_A12 K7
H_DDR2_A13 N3
H_DDR2_A14 N7
H_DDR2_A15 J7

B3 H_DDR2_D30
C7 H_DDR2_D24
C2 H_DDR2_D31
C8 H_DDR2_D26
E3 H_DDR2_D27
E8 H_DDR2_D25
D2 H_DDR2_D29
E7 H_DDR2_D28
B7 H_DDR2_DQM3
A7 H_DDR2_DQS3
C3 H_DDR2_DQSN3
D3 H_DDR2_DQSN3

DM/TDQS
TDQS
DQS
DQS

NC.1
NC.2
NC.3
NC.4
NC.5

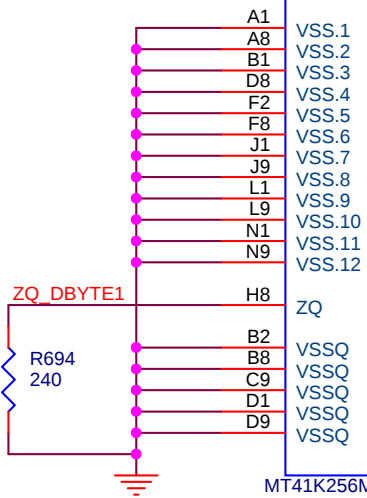
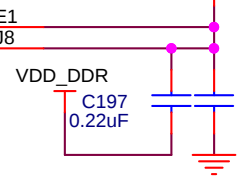
H_DDR2_BA0 J2
H_DDR2_BA1 K8
H_DDR2_BA2 J3

H_DDR2_RASn F3
H_DDR2_CASn G3
H_DDR2_WEn H3
H_DDR2_ODT0 G1
H_DDR2_CKE G9
H_DDR2_CSN0 H2

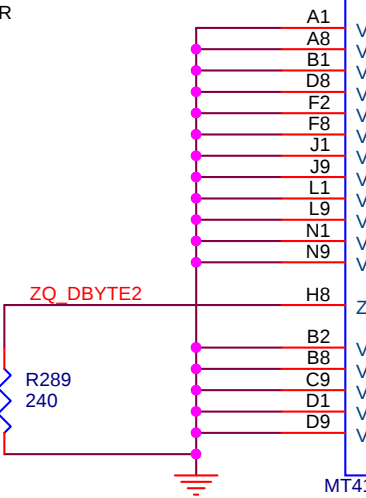
H_DDR2_CLK0 F7
H_DDR2_CLK0NG7

H_DDR2_RST N2

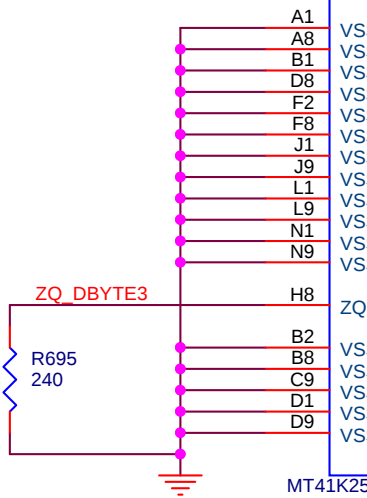
VREFDQ
VREFCA



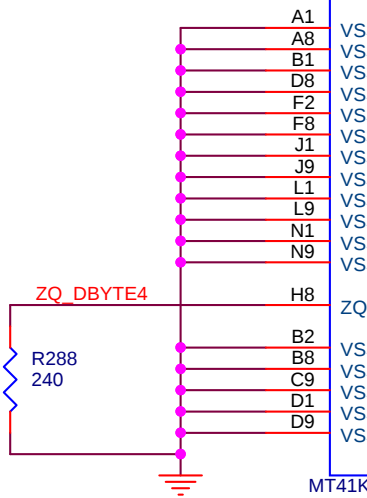
MT41K256M8DA-15E:M ATT



MT41K256M8DA-15E:M ATT



MT41K256M8DA-15E:M ATT



MT41K256M8DA-15E:M ATT

9,30,33 H_DDR2_A0
9,30,33 H_DDR2_A1
9,30,33 H_DDR2_A2
9,30,33 H_DDR2_A3
9,30,33 H_DDR2_A4
9,30,33 H_DDR2_A5
9,30,33 H_DDR2_A6
9,30,33 H_DDR2_A7
9,30,33 H_DDR2_A8
9,30,33 H_DDR2_A9
9,30,33 H_DDR2_A10
9,30,33 H_DDR2_A11
9,30,33 H_DDR2_A12
9,30,33 H_DDR2_A13
9,30,33 H_DDR2_A14
9,30,33 H_DDR2_A15

9,30,33 H_DDR2_RASN
9,30,33 H_DDR2_CASN
9,30,33 H_DDR2_WEN
9,30,33 H_DDR2_ODT0
9,30,33 H_DDR2_CKE
9,30,33 H_DDR2_CSN0
9,30,33 H_DDR2_CLK0
9,30,33 H_DDR2_CLK0N

9 H_DDR2_D0
9 H_DDR2_D1
9 H_DDR2_D2
9 H_DDR2_D3
9 H_DDR2_D4
9 H_DDR2_D5
9 H_DDR2_D6
9 H_DDR2_D7
9 H_DDR2_D8
9 H_DDR2_D9
9 H_DDR2_D10
9 H_DDR2_D11
9 H_DDR2_D12
9 H_DDR2_D13
9 H_DDR2_D14
9 H_DDR2_D15

9 H_DDR2_D16
9 H_DDR2_D17
9 H_DDR2_D18
9 H_DDR2_D19
9 H_DDR2_D20
9 H_DDR2_D21
9 H_DDR2_D22
9 H_DDR2_D23
9 H_DDR2_D24
9 H_DDR2_D25
9 H_DDR2_D26
9 H_DDR2_D27
9 H_DDR2_D28
9 H_DDR2_D29
9 H_DDR2_D30
9 H_DDR2_D31

9,30,33 H_DDR2_BA0
9,30,33 H_DDR2_BA1
9,30,33 H_DDR2_BA2

9 H_DDR2_DQM0
9 H_DDR2_DQS0
9 H_DDR2_DQSN0

9 H_DDR2_DQM2
9 H_DDR2_DQS2
9 H_DDR2_DQSN2

9 H_DDR2_RST

9 H_DDR2_DQM1
9 H_DDR2_DQS1
9 H_DDR2_DQSN1

9 H_DDR2_DQM3
9 H_DDR2_DQS3
9 H_DDR2_DQSN3

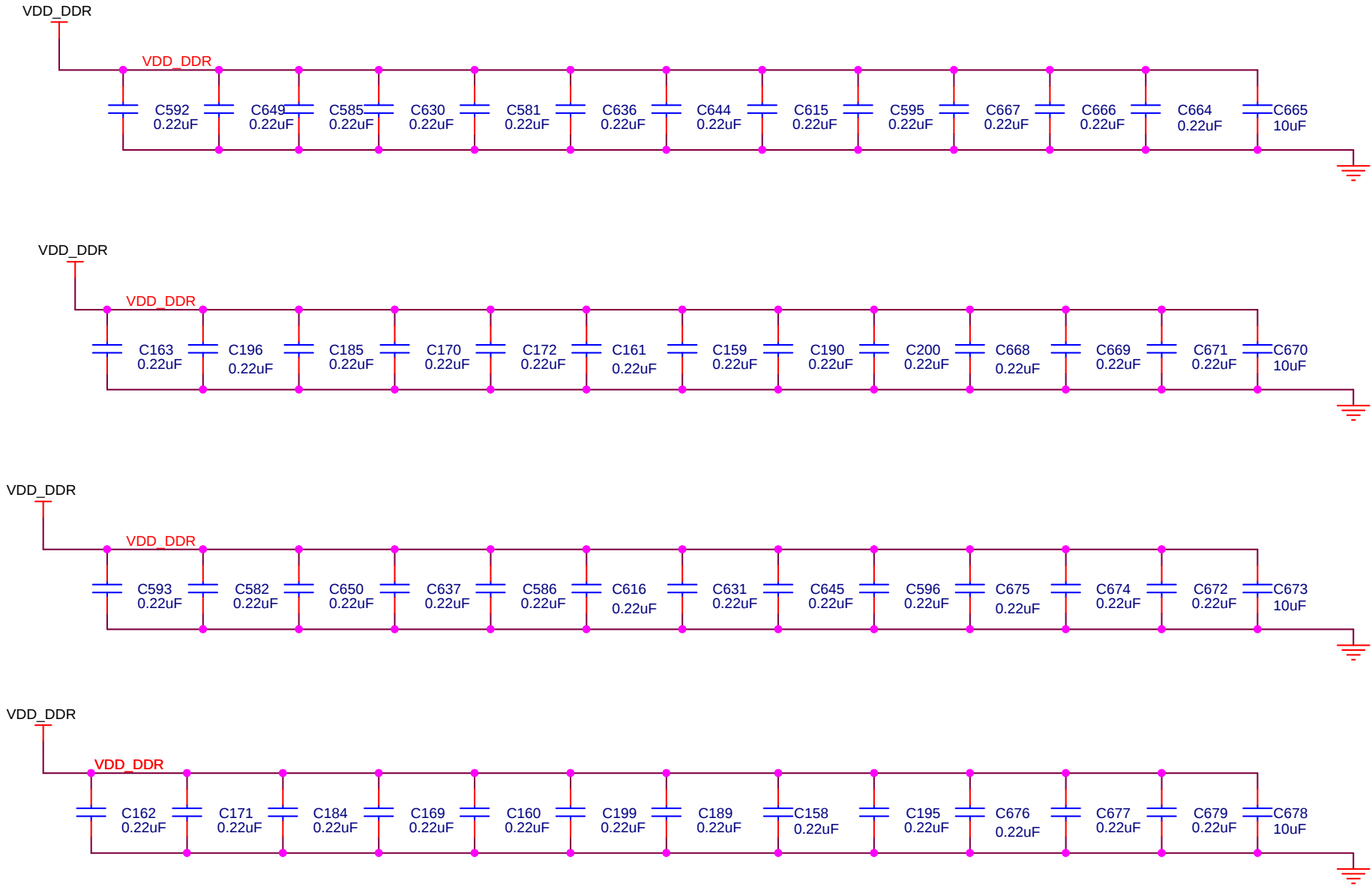
CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR3 EMIF2 Bank2			
Size:B	DWG NO	tdb	Revision: A
Date: Tuesday, December 10, 2013			Sheet 31 of 58

Preliminary Information - Subject to change

Auto Cap Sizes Updated

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

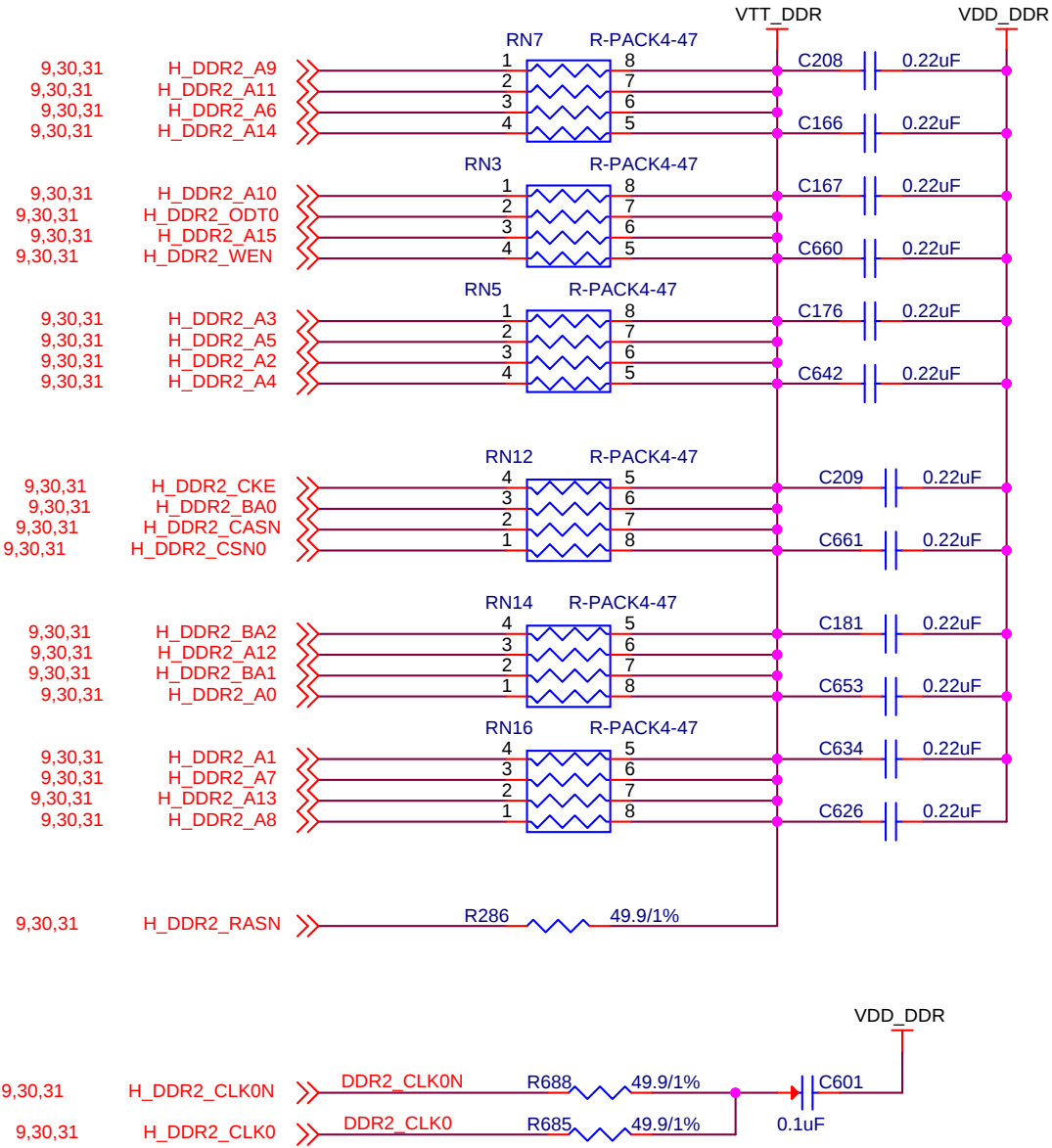
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED		
Title: Virtual J6 DRI Board		
Page Contents: Vayu DDR3 Bank2 Caps		
Size:B	DWG NO tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 32 of	58

TI CONFIDENTIAL - NDA RESTRICTIONS

Auto Cap Sizes Updated

Work - In - Progress



CAPACITANCE	Commerical	Automotive
Vaule	Size/X5R	Size/X7R
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

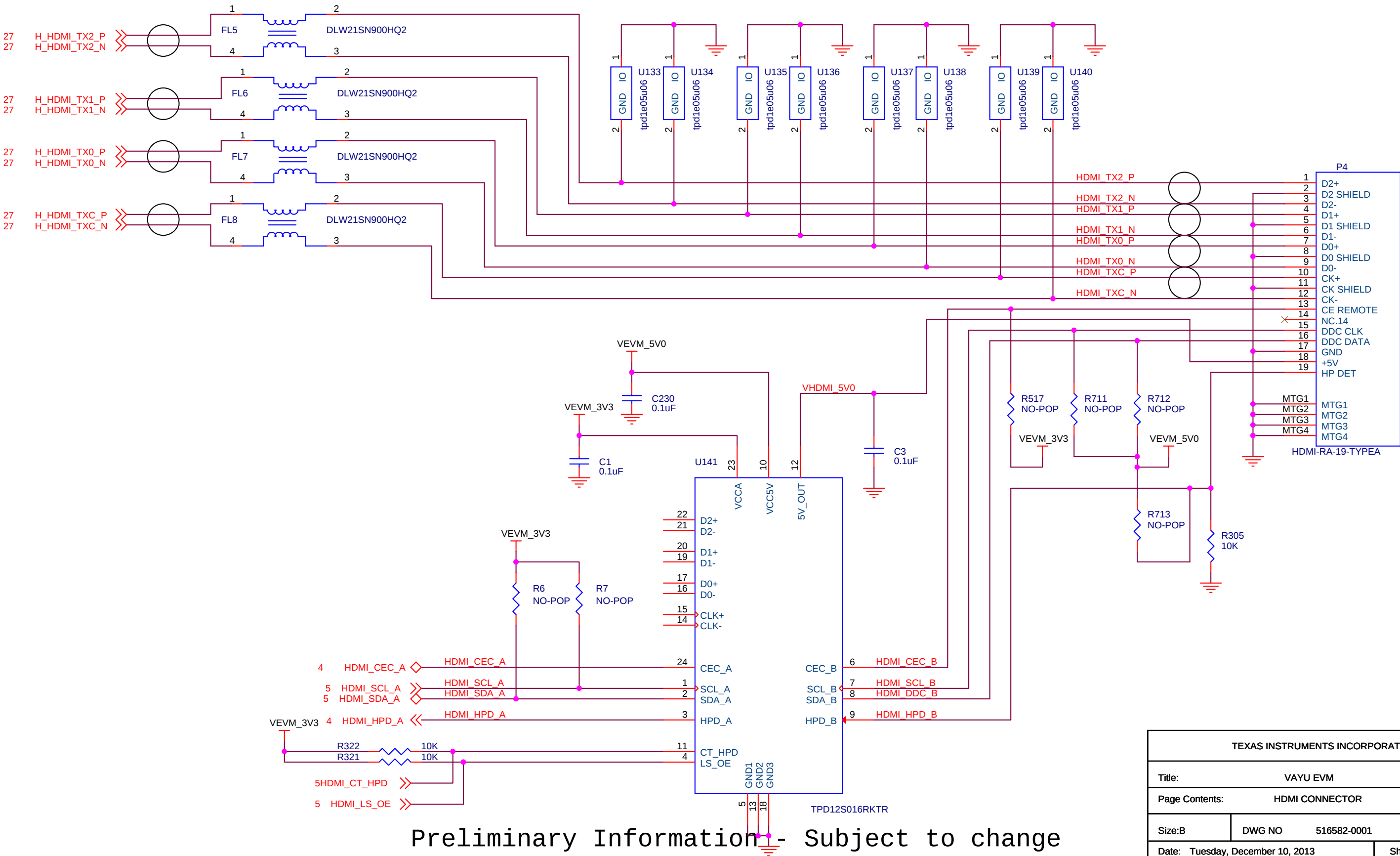
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu DDR3 EMIF2 Terminations			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 33 of		58

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

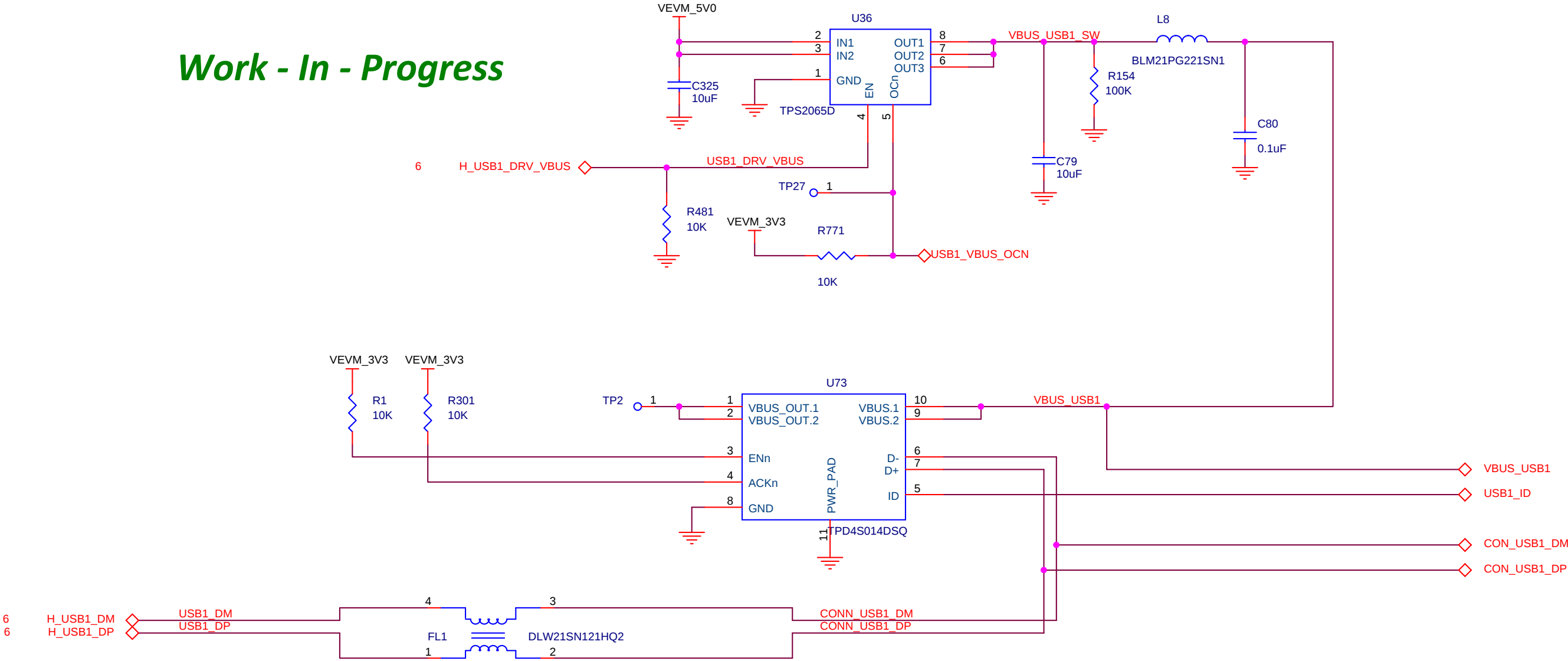
Work - In - Progress

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



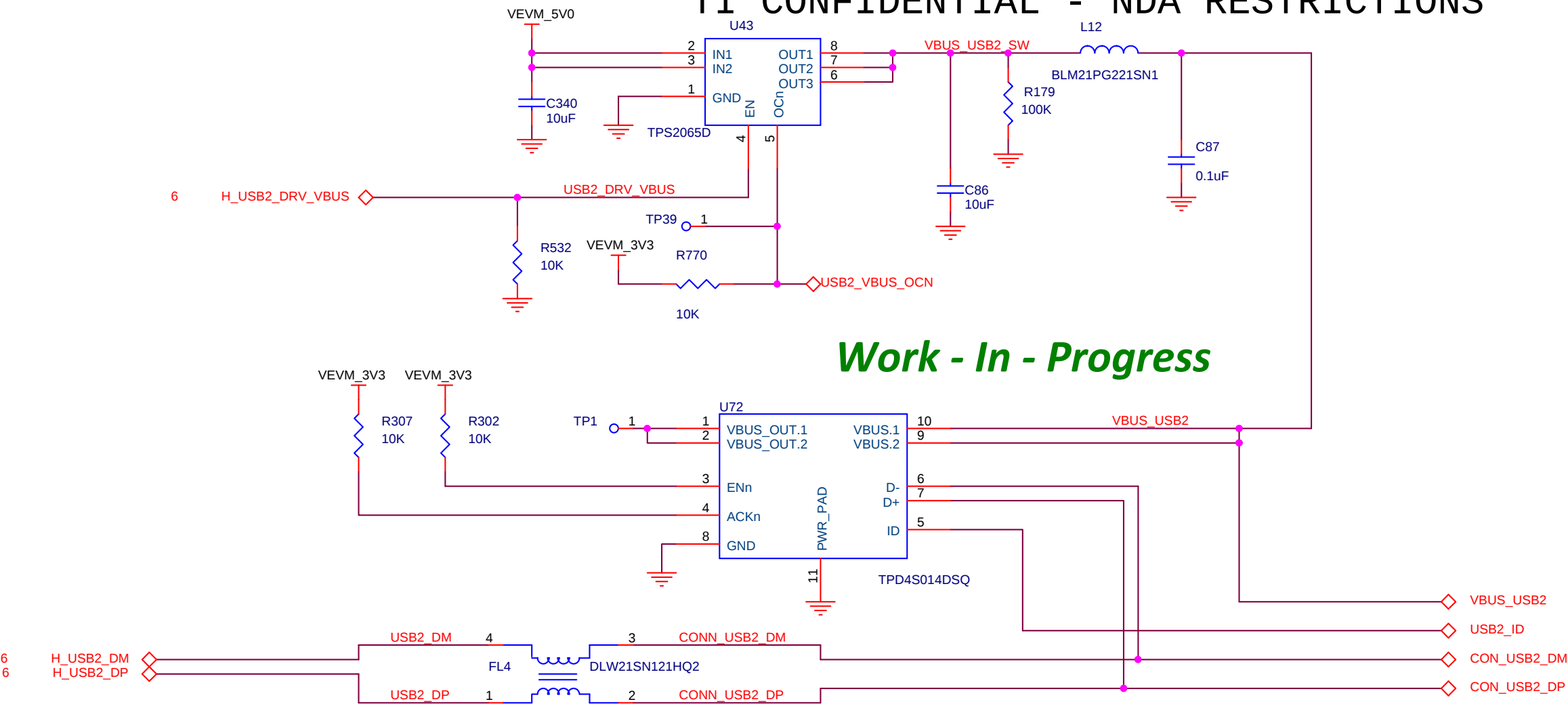
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: HDMI CONNECTOR			
Size: B	DWG NO	516582-0001	Revision: E
Date: Tuesday, December 10, 2013		Sheet 34 of	58

Work - In - Progress



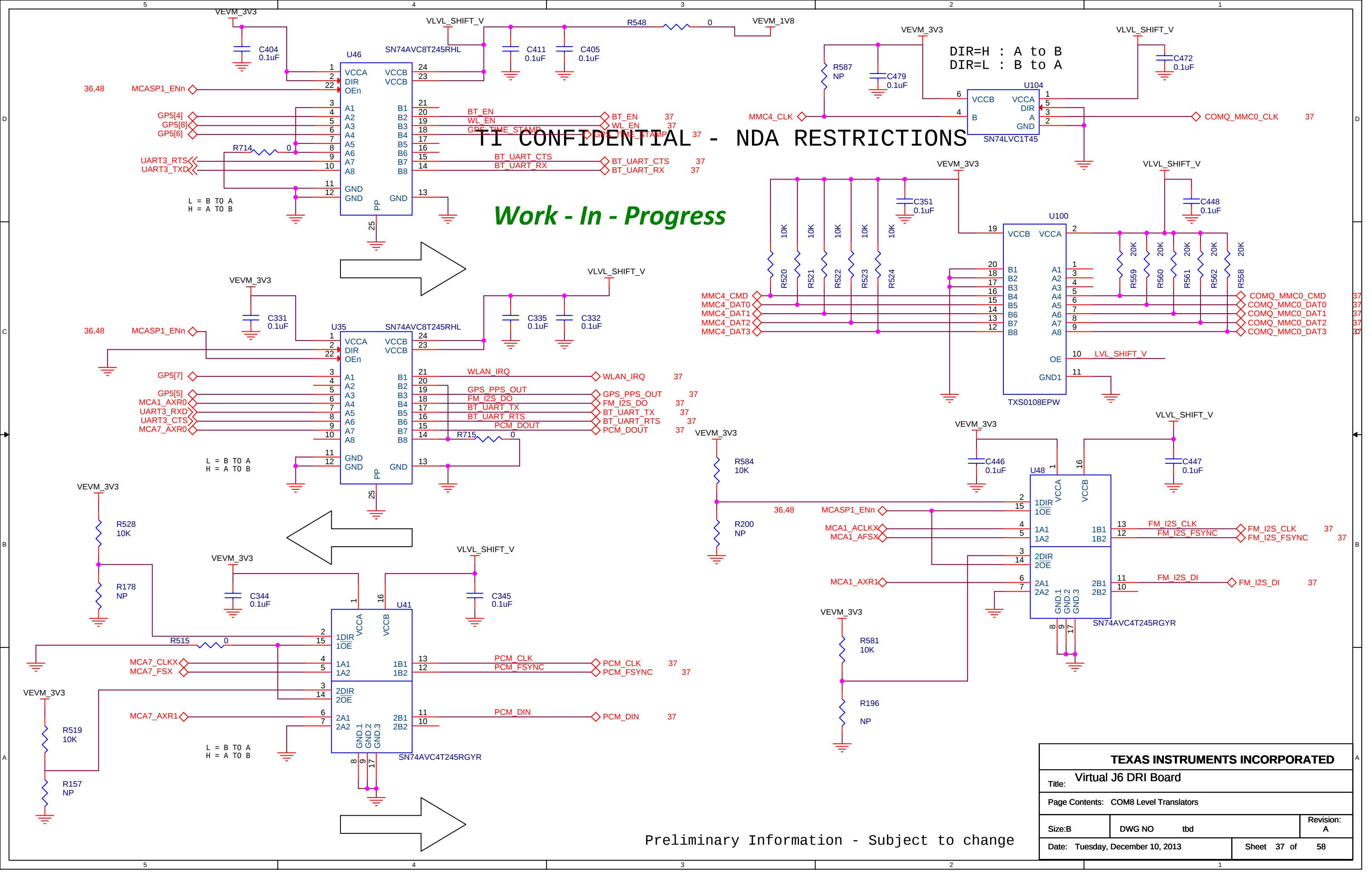
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: USB1			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 35 of 58		



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Vayu USB2			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 36 of		58



TI CONFIDENTIAL - NDA RESTRICTIONS

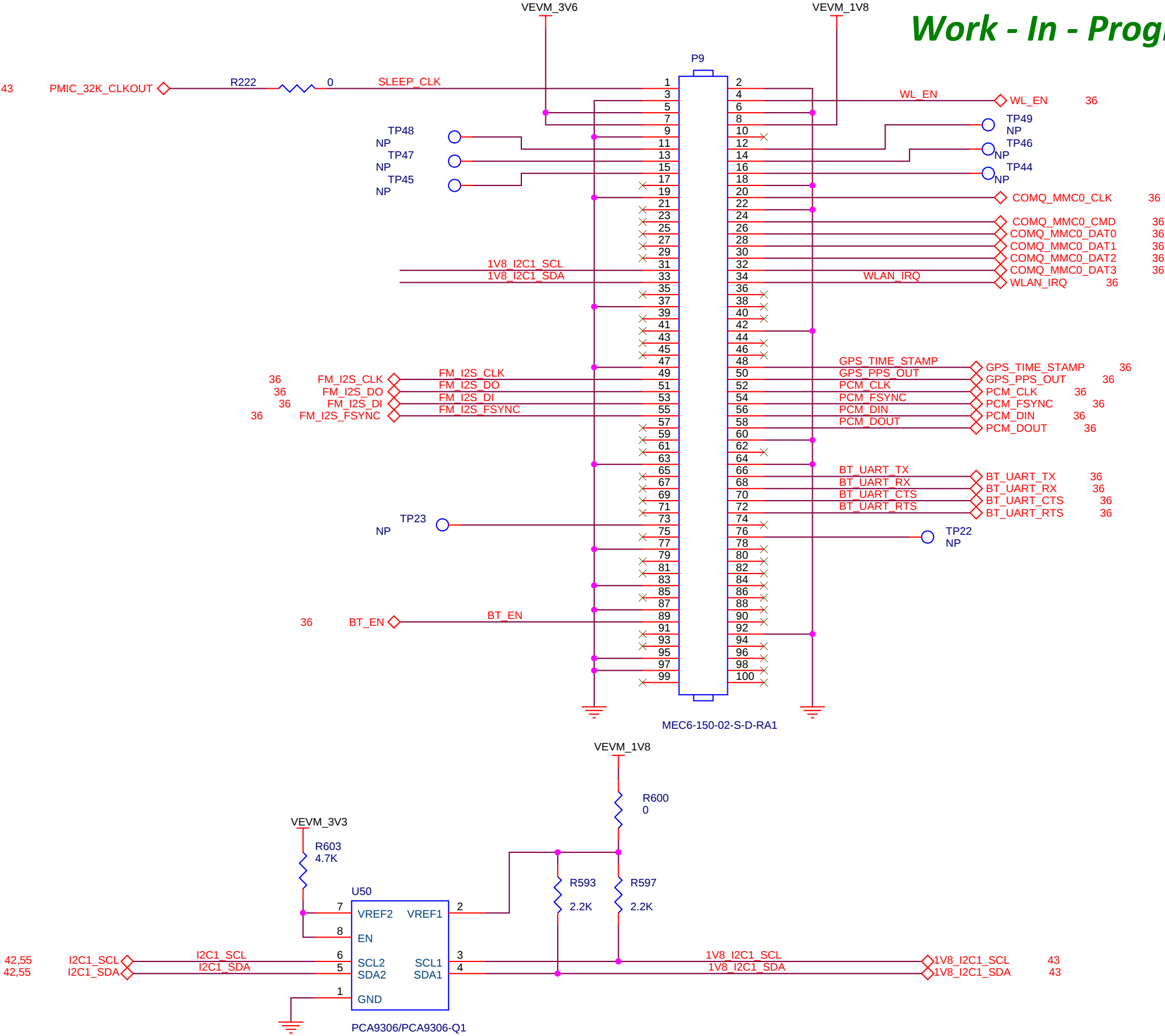
Work - In - Progress

DIR=H : A to B
DIR=L : B to A

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: COM8 Level Translators			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013			Sheet 37 of 58

Preliminary Information - Subject to change

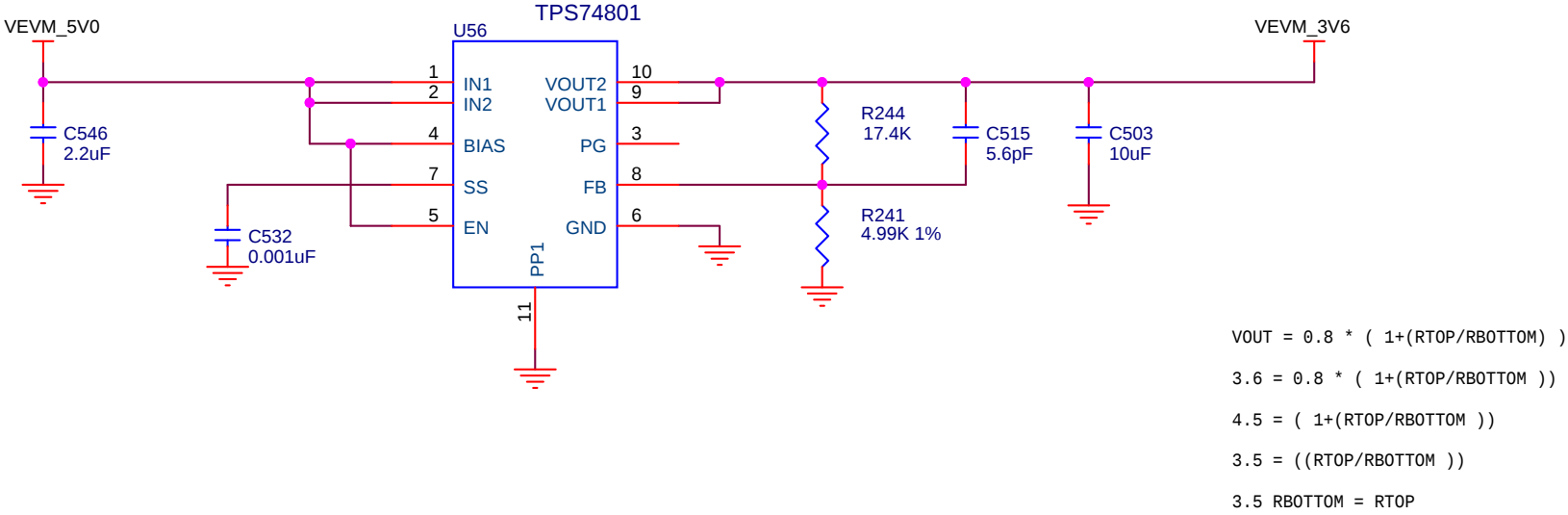
Work - In - Progress



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: COM8 Connector			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet	38 of	58

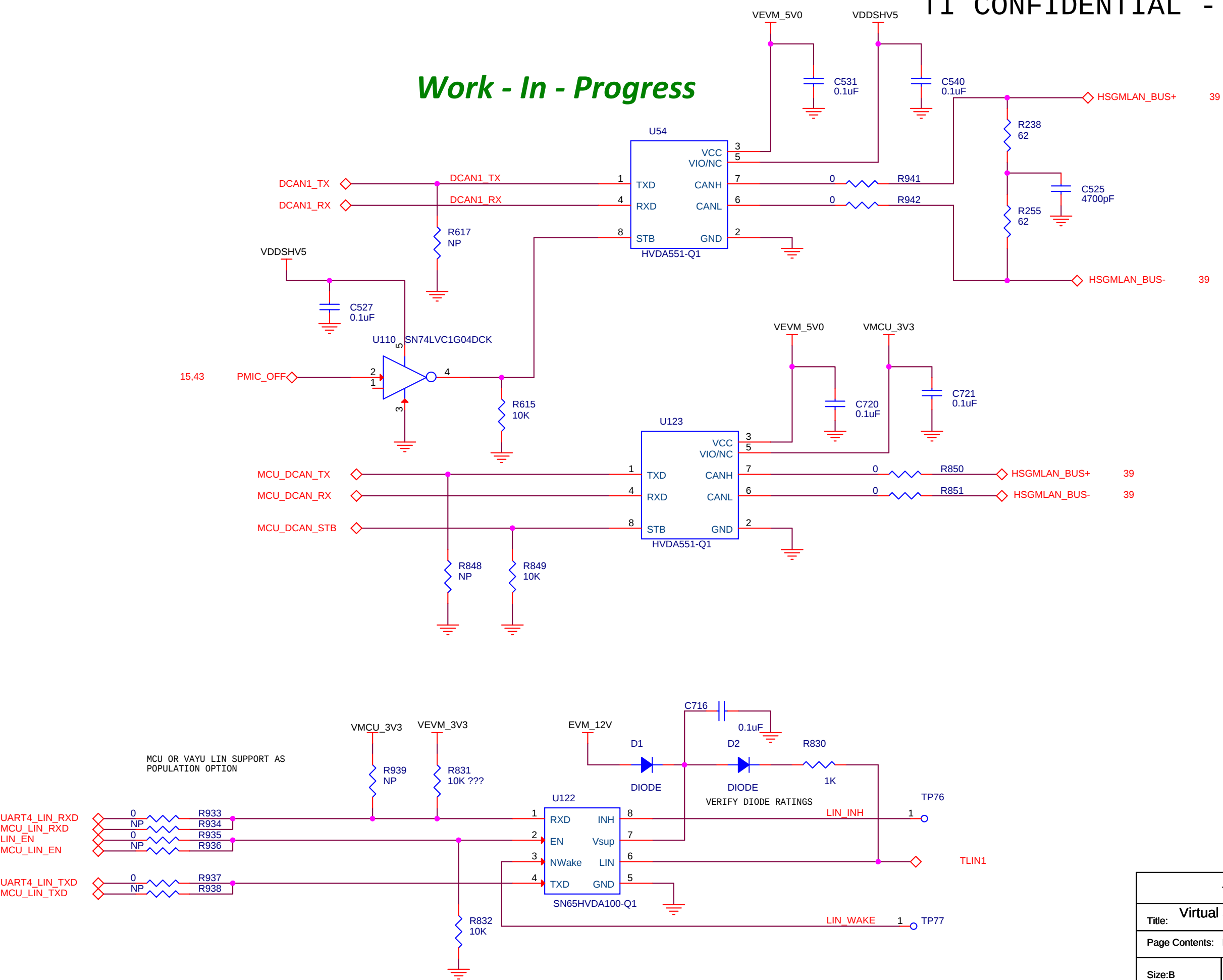
Work - In - Progress



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: COM8 Power			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 39 of		58

Work - In - Progress

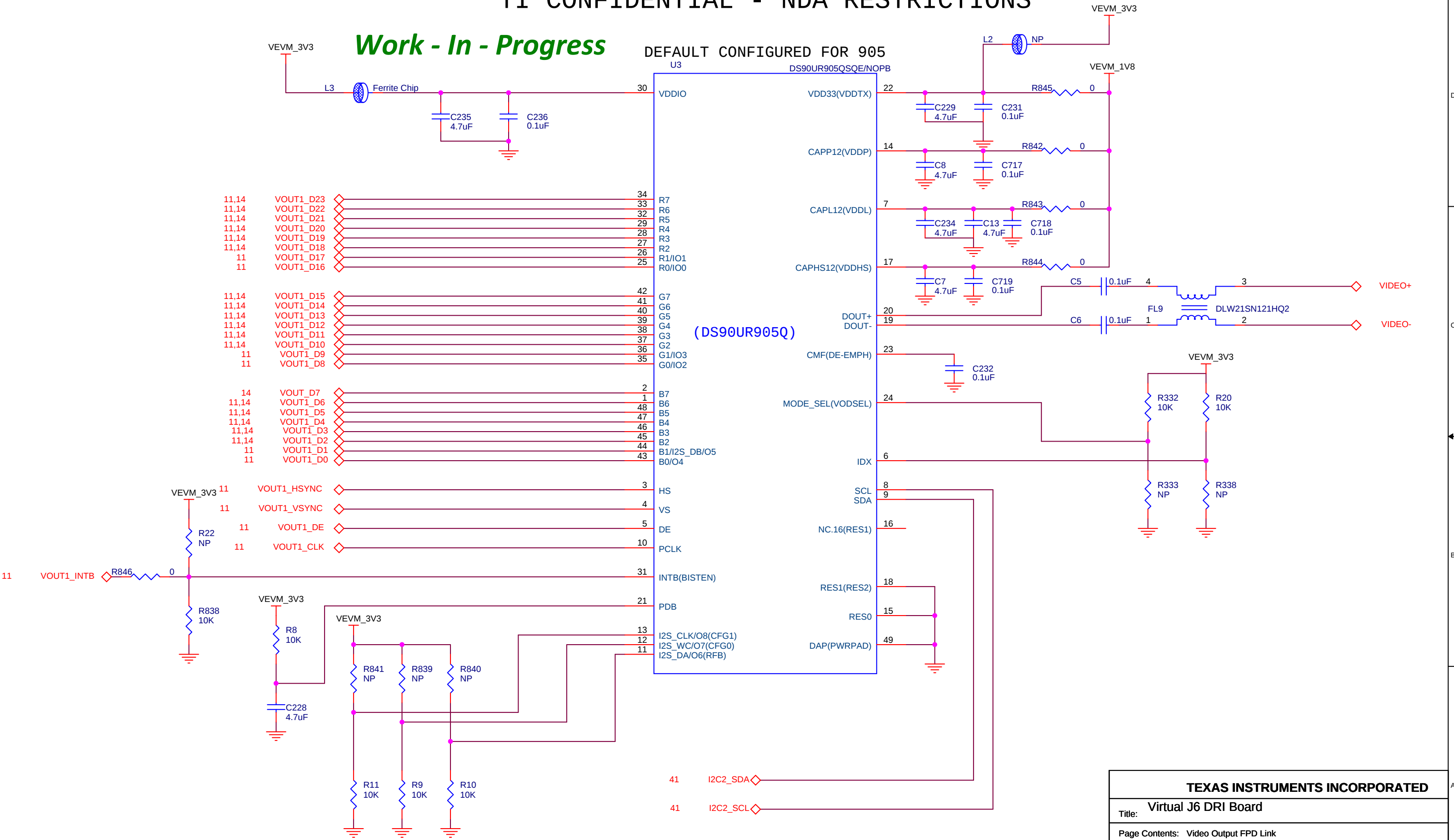


Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: DCAN1-2			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013		Sheet 40 of	58

Work - In - Progress

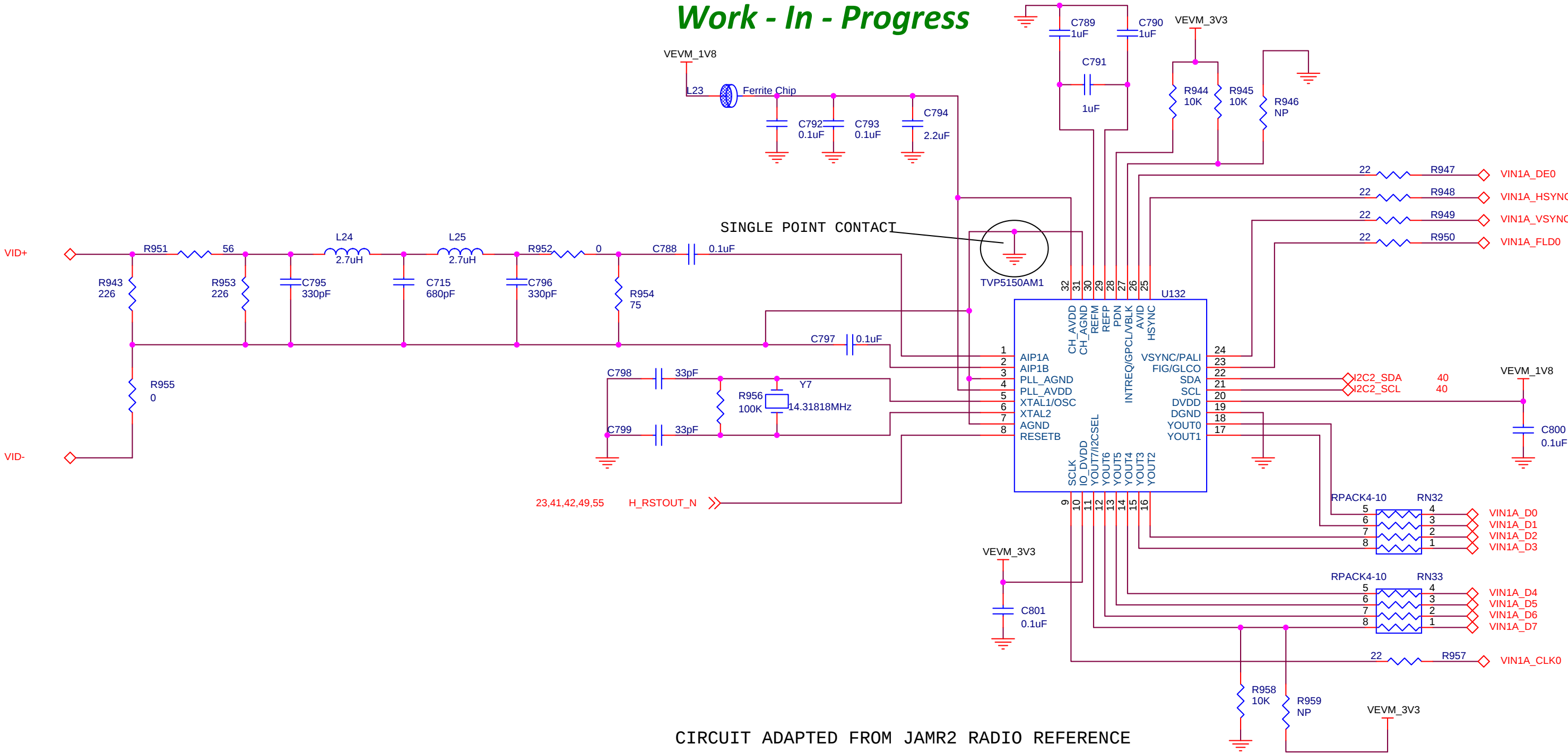
DEFAULT CONFIGURED FOR 905



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Video Output FPD Link			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 41 of		58

Work - In - Progress

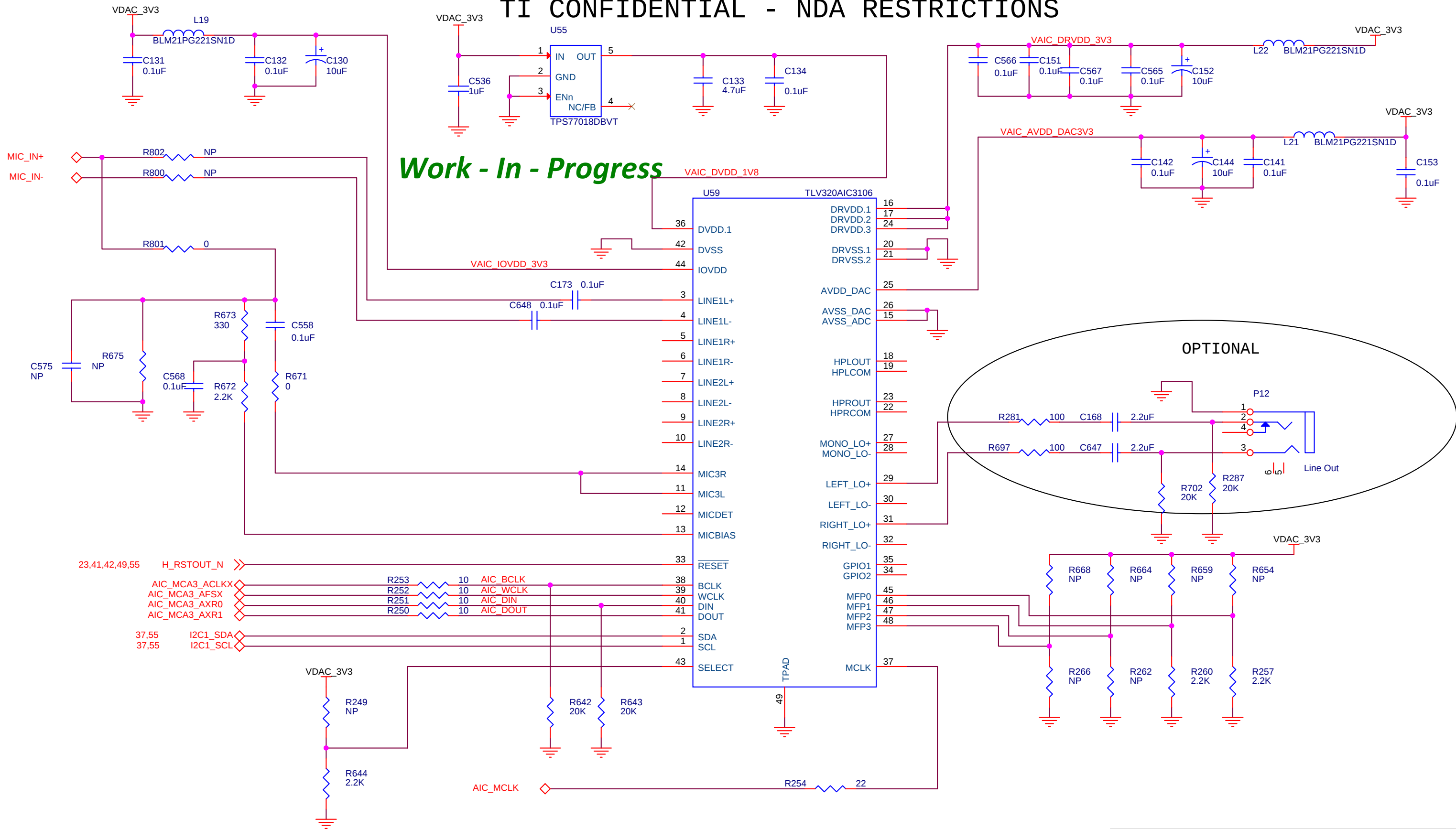


CIRCUIT ADAPTED FROM JAMR2 RADIO REFERENCE

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Video Input			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013		Sheet 42 of	58

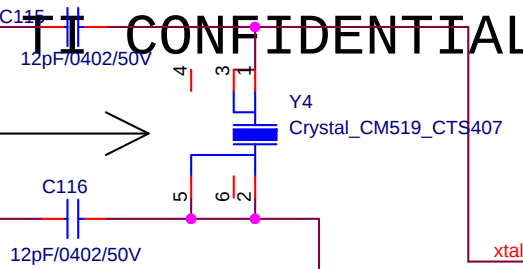
Work - In - Progress



TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Audio Co-Dec			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 43 of 58		

PMIC HAS DUAL FOOTPRINT
FOR 32678 HERTZ AND 16.384
MHZ CRYSTAL

PMIC VIO IS 1.8 VOLTS
NOT THIS MEANS TRANSLATORS FOR I2C AND OTHERS



CONFIDENTIAL - NDA RESTRICTIONS

TPS659039

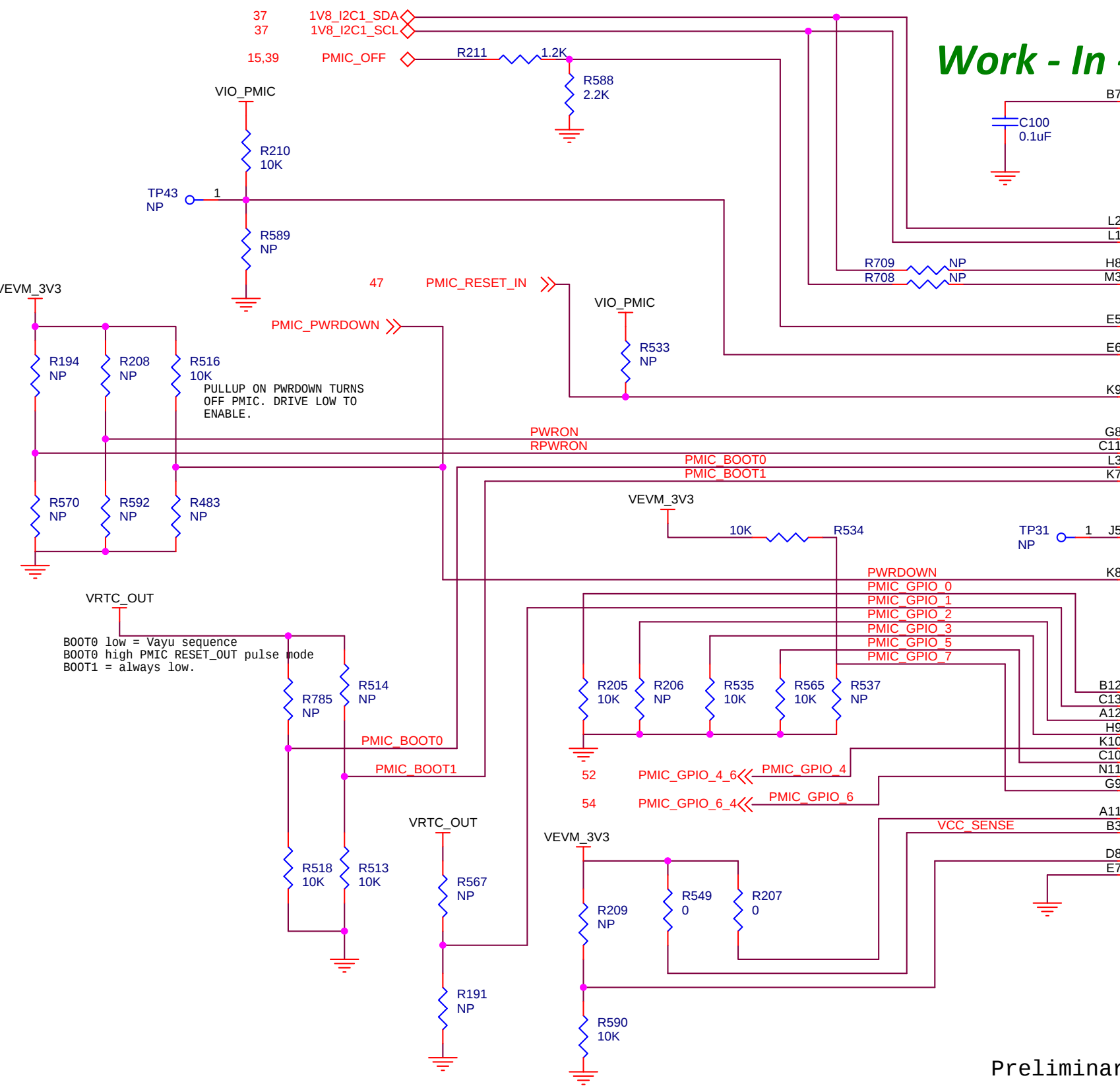
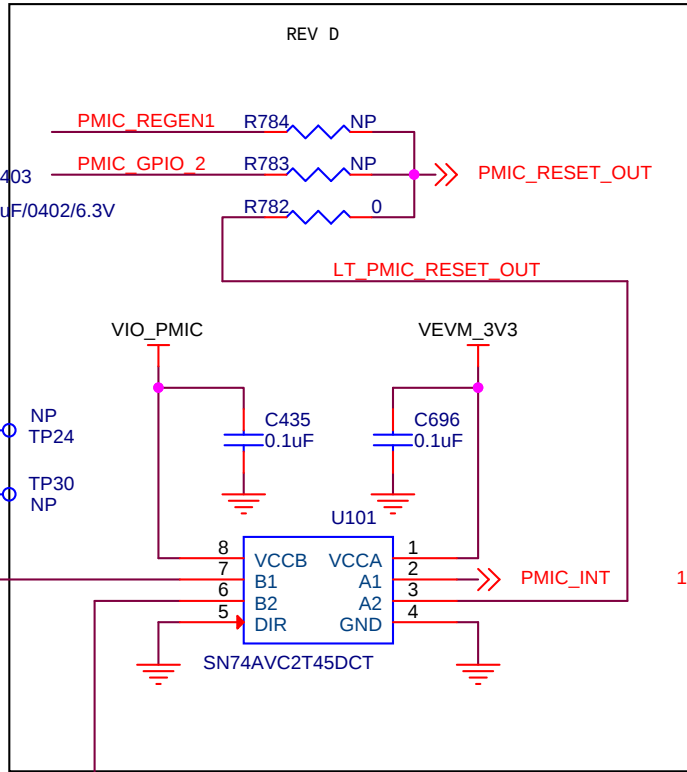
CLOCK

REFERENCE

Work - In - Progress

CONTROL

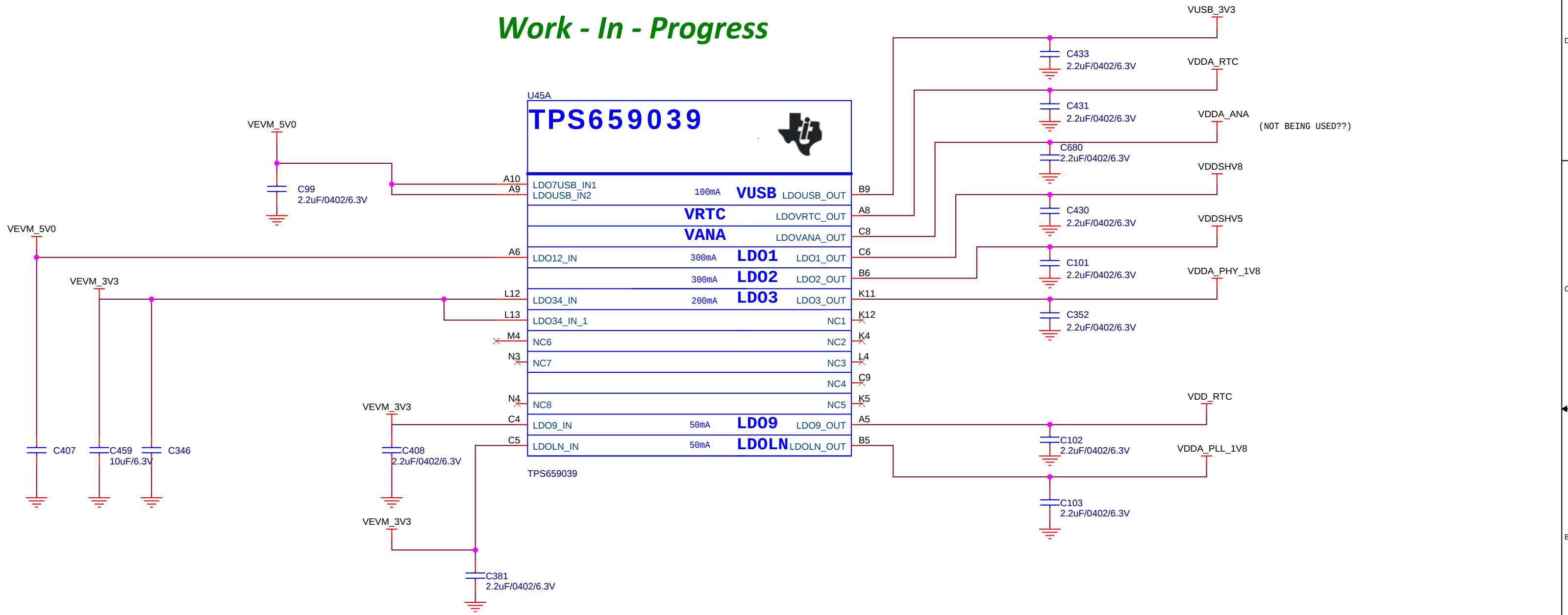
TEST



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: PMIC Control			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 44 of 58		

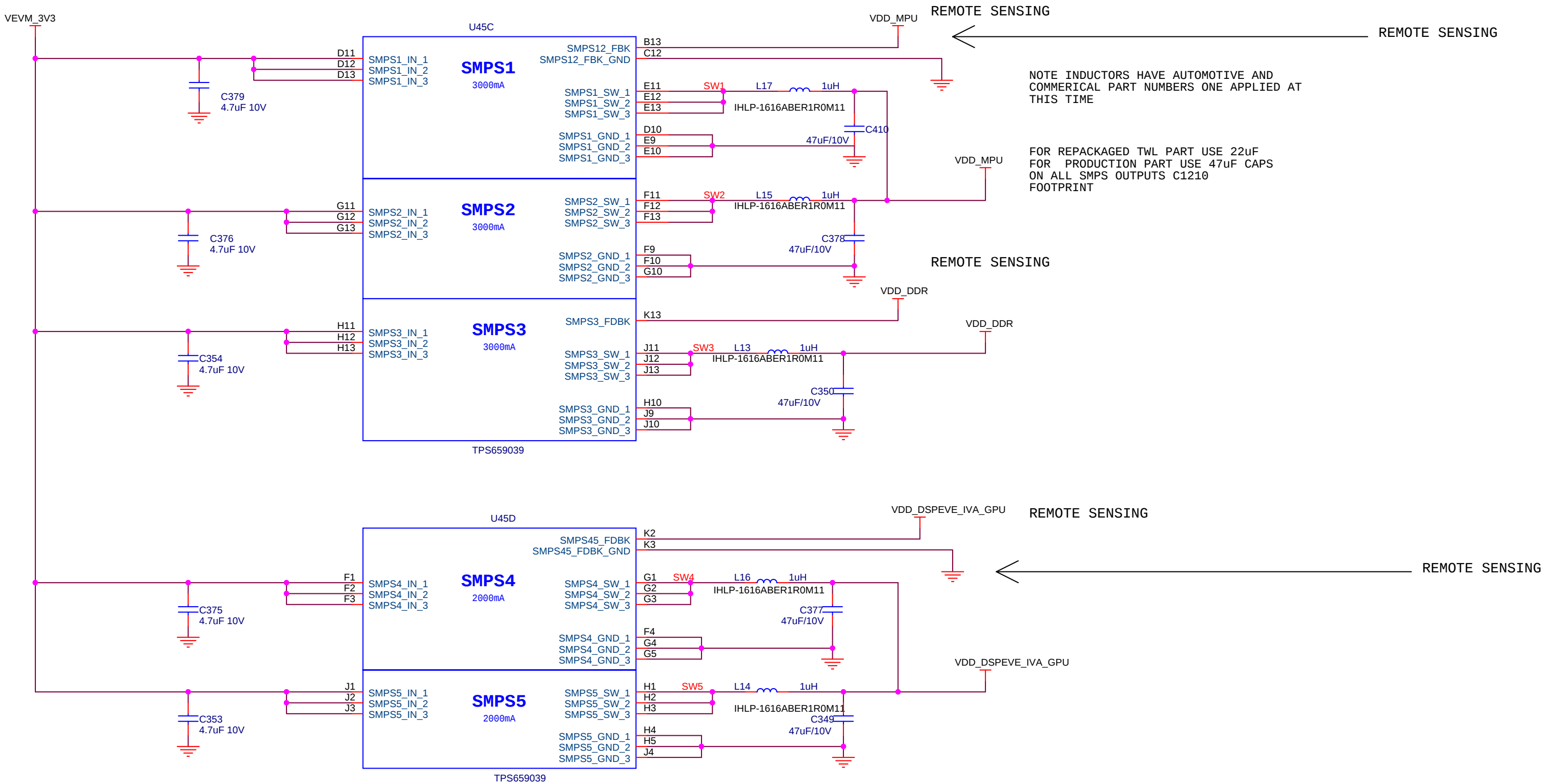
Work - In - Progress



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: PMIC LDOs			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 45 of 58		

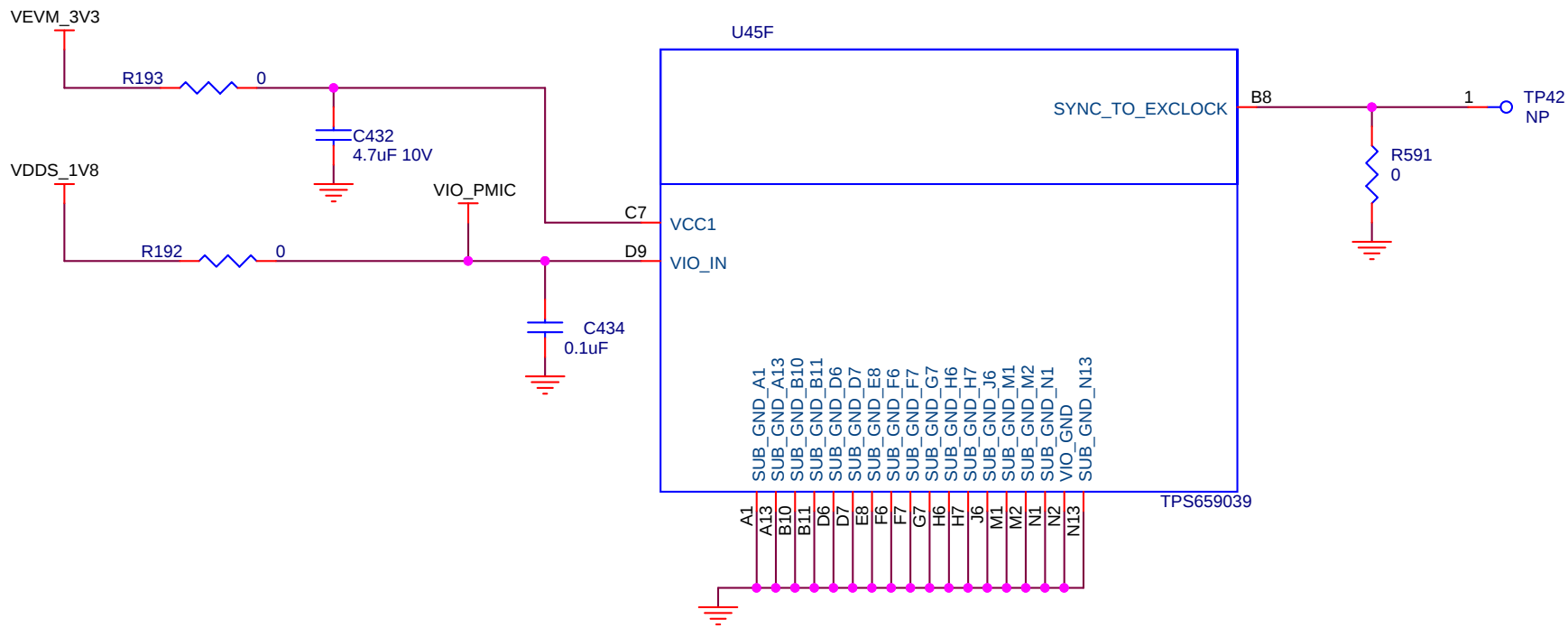
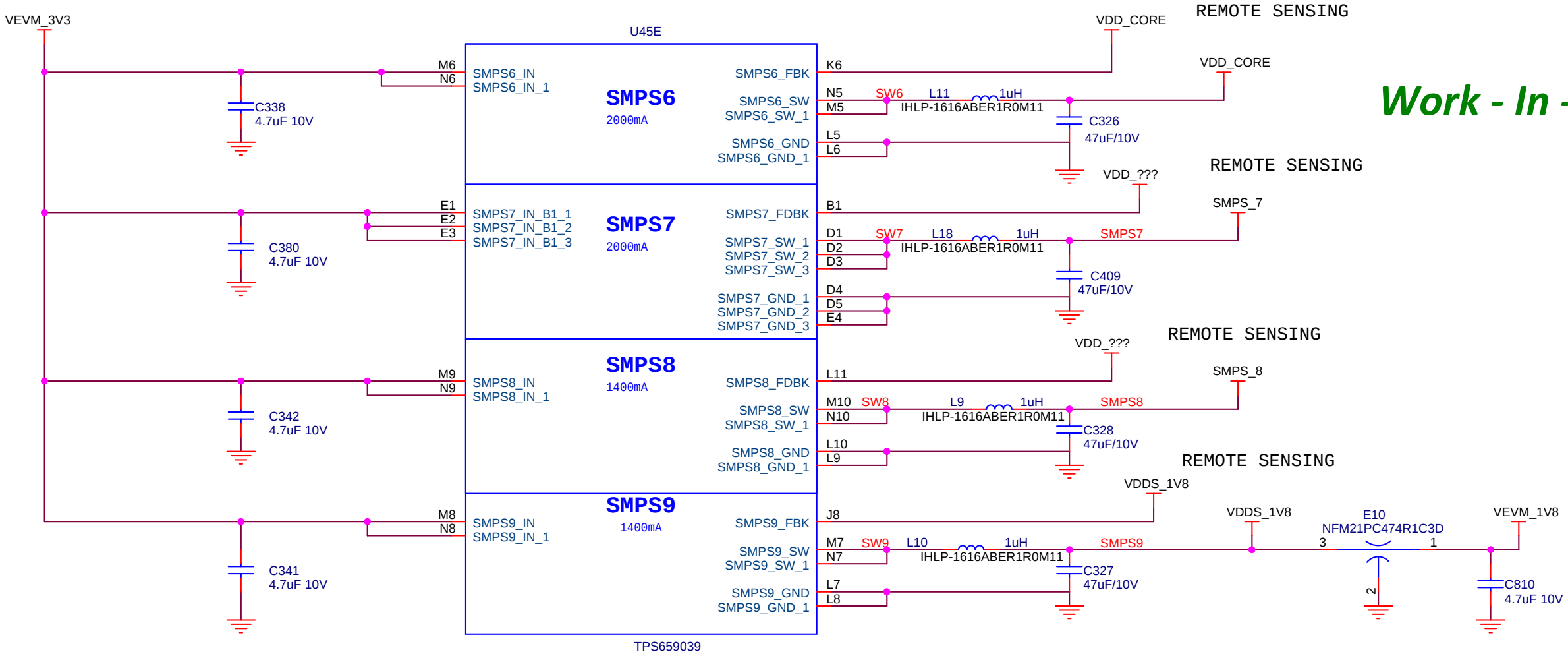
Work - In - Progress



TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: PMIC SMPS1-5			
Size: B	DWG NO	tdb	Revision: A
Date: Tuesday, December 10, 2013	Sheet 46 of 58		

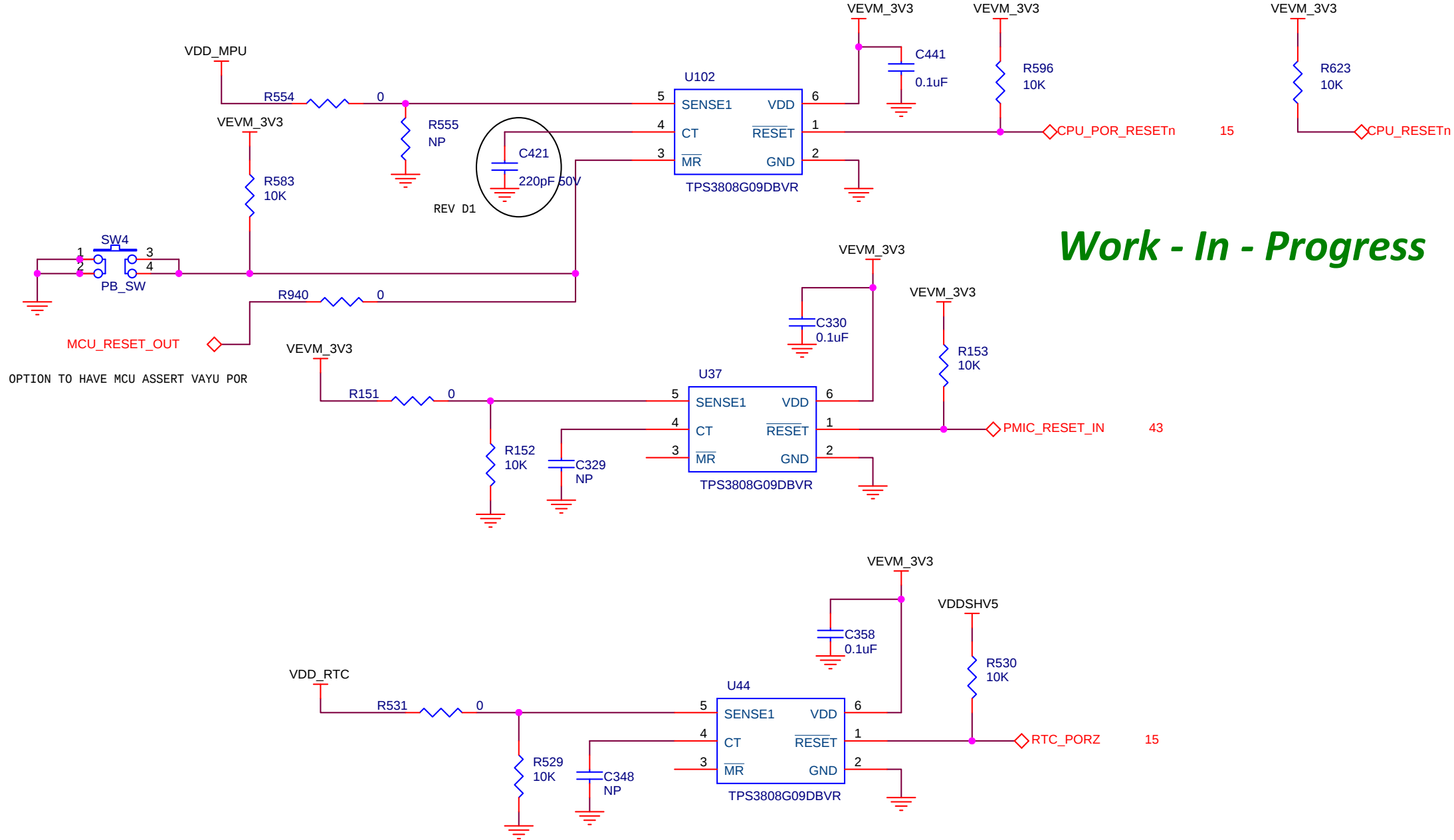
TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress



Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: PMIC			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 47 of		58

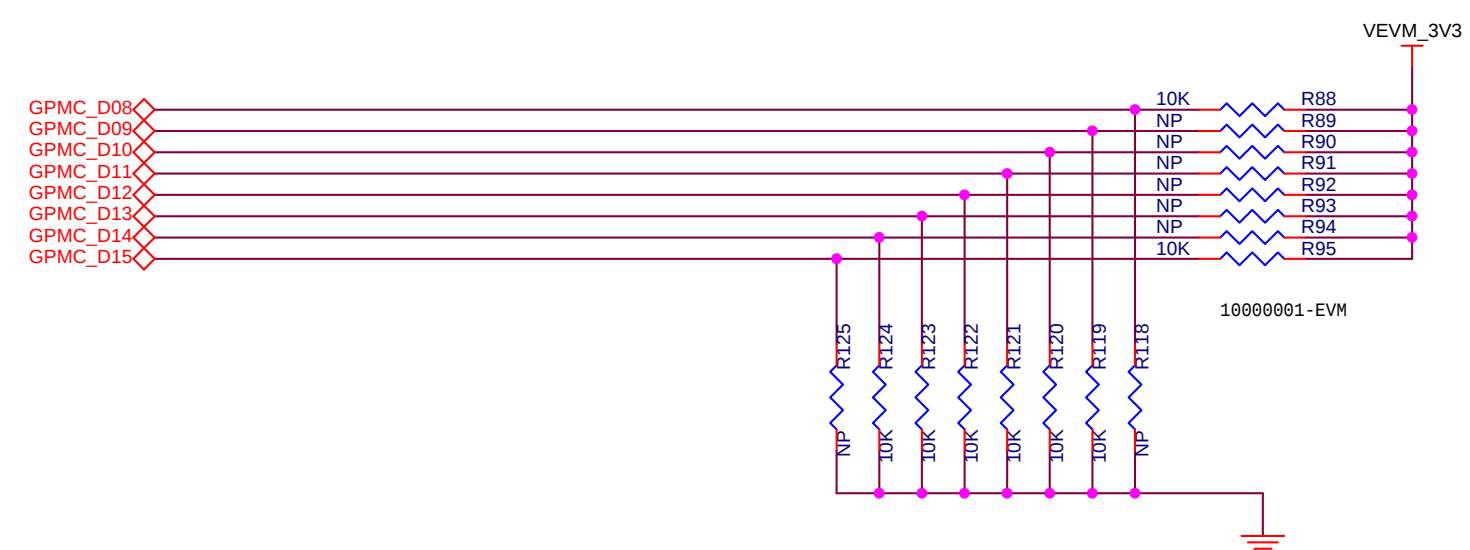
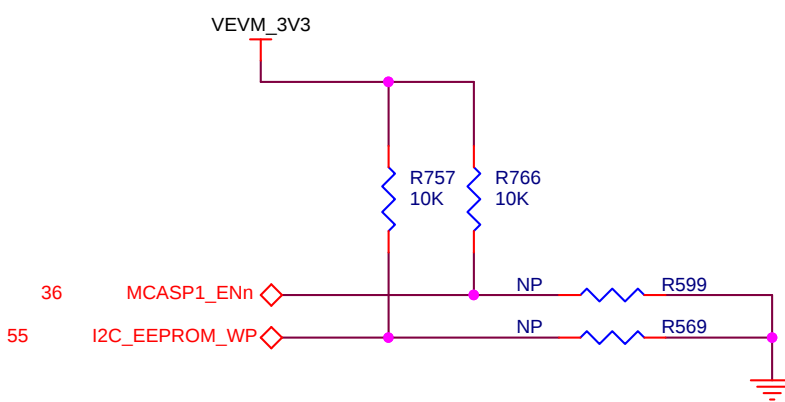
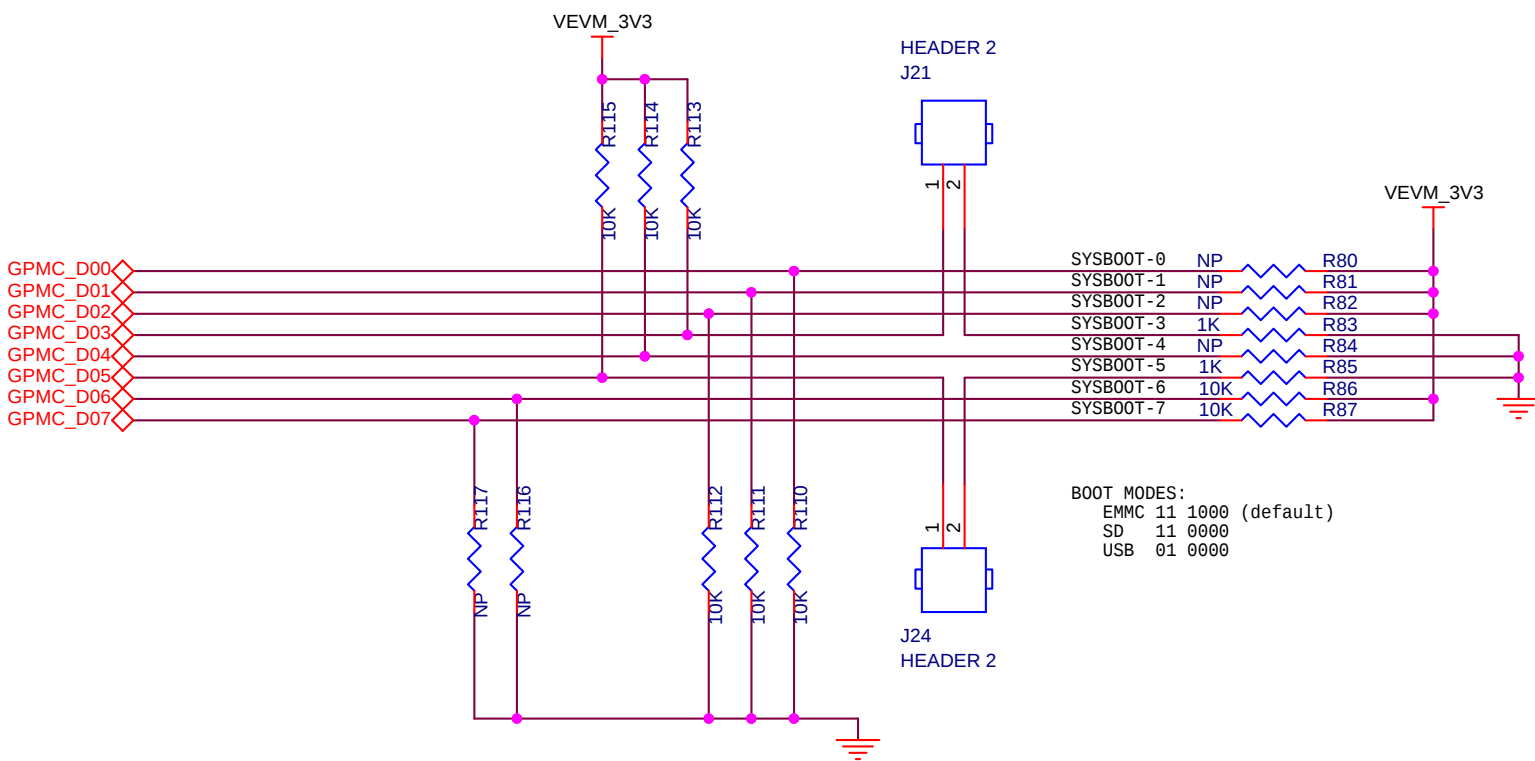


Work - In - Progress

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Reset Generation			
Size: B	DWG NO	tbd	Revision: A
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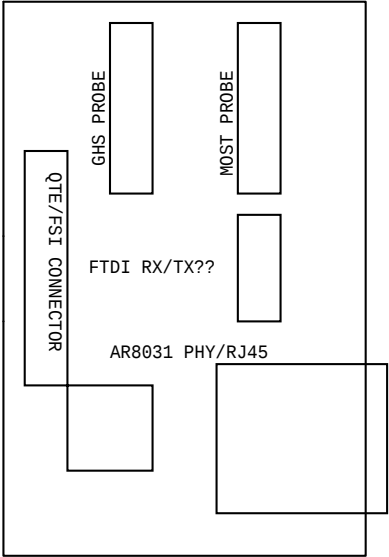
Work - In - Progress



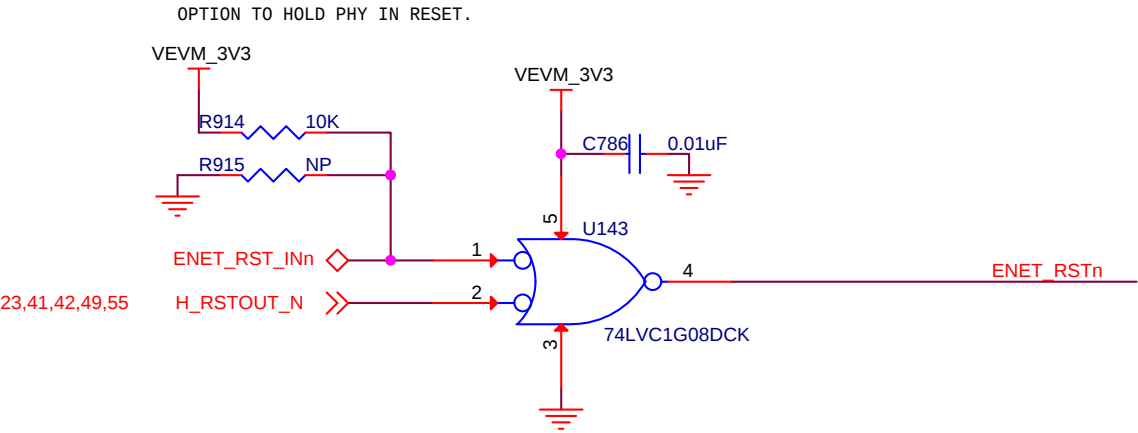
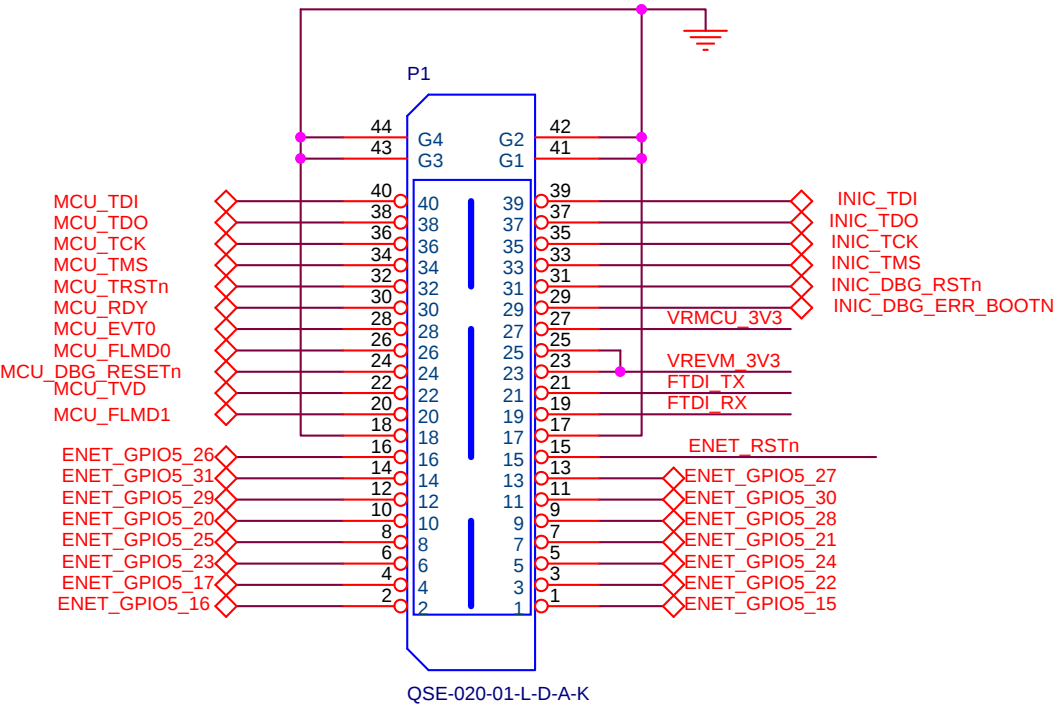
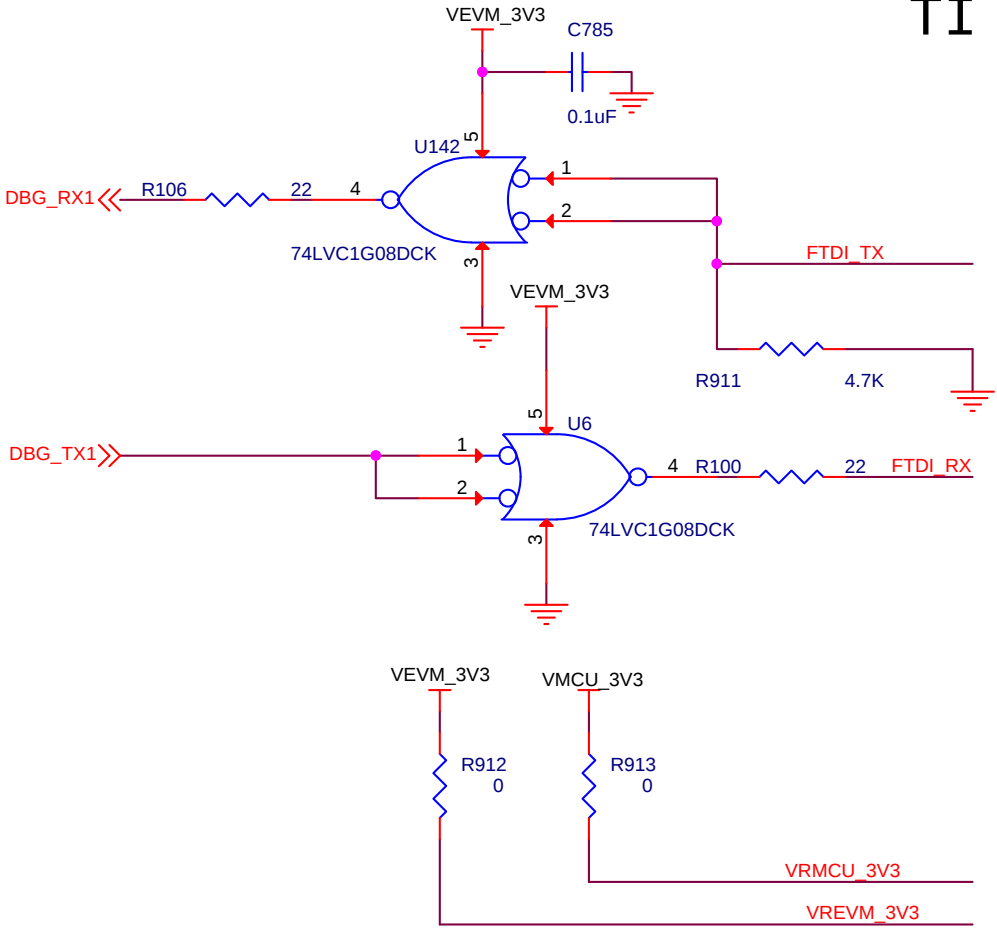
Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: SoC Boot Settings			
Size:B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 49 of		58

Work - In - Progress

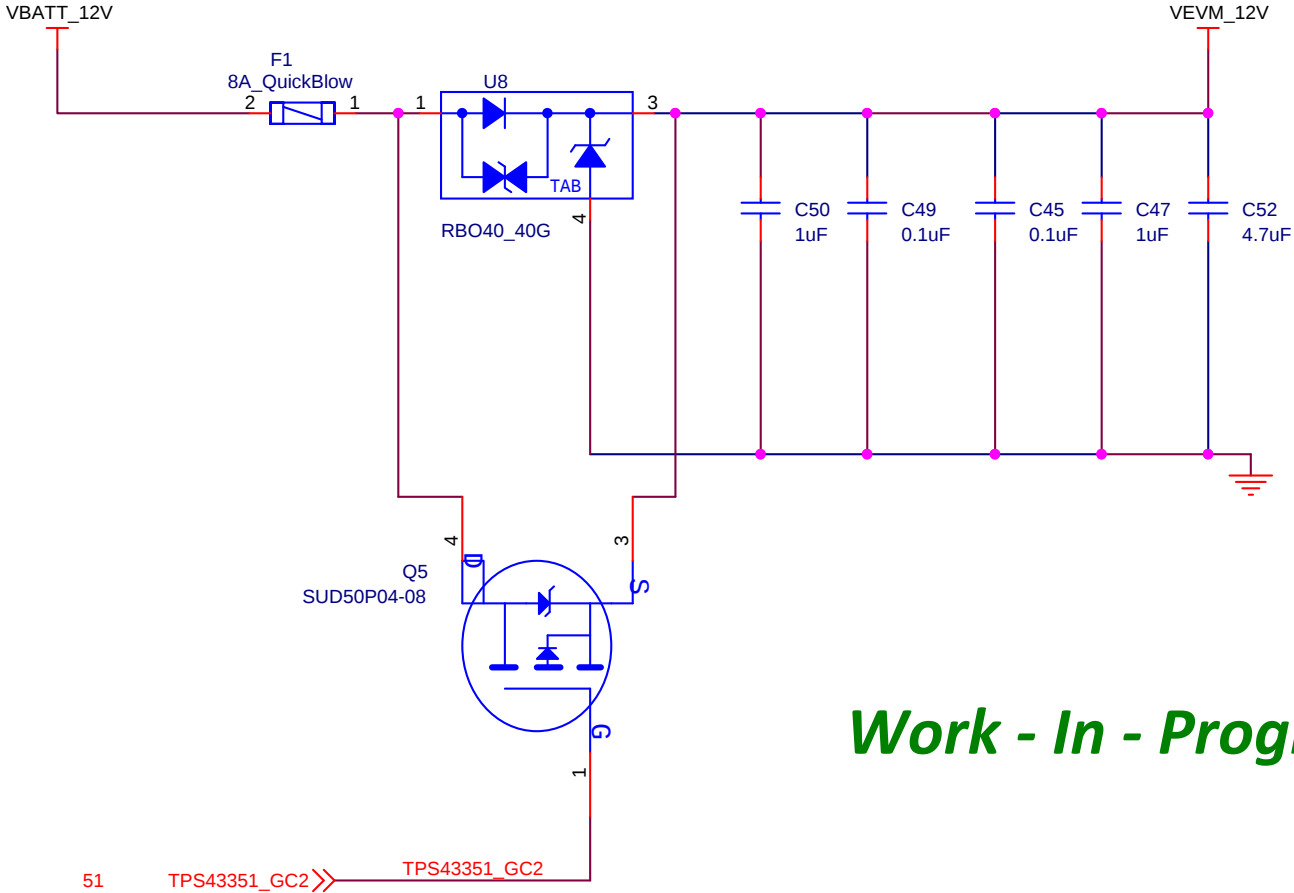


DEBUG ADAPTER



PLAN IS TO CONNECT RGMII TO AN AR8031 PHY IN RGMII MODE. IF WE RUN INTO SIGNAL ISSUES THEN WILL DOWNGRADE TO MII.

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Debug			
Size:B	DWG NO	tbd	Revision: A
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Work - In - Progress

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power Input			
Size: B	DWG NO	tbd	Revision: A
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TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

VBATT_12V VEVM_12V

TPS43351_GC2 TPS43351_GC2 50

C51 100uF,16V

U23 TPS43351QDAPRQ1

GA1 GA2 GA1 GA2

PHA PHA PHA PHA

SA1 SA2 SA1 SA2

FBA FBA FBA FBA

COMPA COMPA COMPA COMPA

PGA PGA PGA PGA

C300 .22uF,50V

R451 10

R457 10

C302 0.01uF

C307 2700pF

R464 15K

C309 56pf

R140 10k

C299 .22uF,50V

GB1 GB2 GB1 GB2

PHB PHB PHB PHB

SB1 SB2 SB1 SB2

FBB FBB FBB FBB

COMPB COMPB COMPB COMPB

PGB PGB PGB PGB

VEVM_3V3 VEVM_3V3 VEVM_3V3 VEVM_3V3

R140 10k

C301 0.01uF

C303 2000pF

R461 20K

C304 39pf

VEVM_5V0 VEVM_5V0 VEVM_5V0 VEVM_5V0

R138 10k

VEVM_12V VEVM_12V VEVM_12V VEVM_12V

C62 22uF,25V, x5R

C60 330pF

C63 22uF,25V, x5R

C61 330pF

L6 2.2uH (7443330220)

R126 10

L7 8.2uH(744771008)

R127 10

R134 .005 OHM

R135 0.015

C683 100uF 10V

C71 100uF 10V

C74 100uF 10V

C76 100pF

C77 47uF 16V

C72 47uF 16V

C78 100pF

R143 49.9

R144 49.9K 1%

R472 16.0K 1%

R147 49.9

R146 84.5K 1%

R145 16.0K 1%

10TPB100ML 10 Volts Less than ESR 35m-ohm

10 Volts Less than ESR 35m-ohm

GRM32ER61A476KE20L (1210-10V) T525D476M016ATE035 (7343-16V) 100uF total

POSSIBLE HIGHER VOLTAGE RANGE ON C63

10 Volts Less than ESR 35m-ohm

TEXAS INSTRUMENTS INCORPORATED

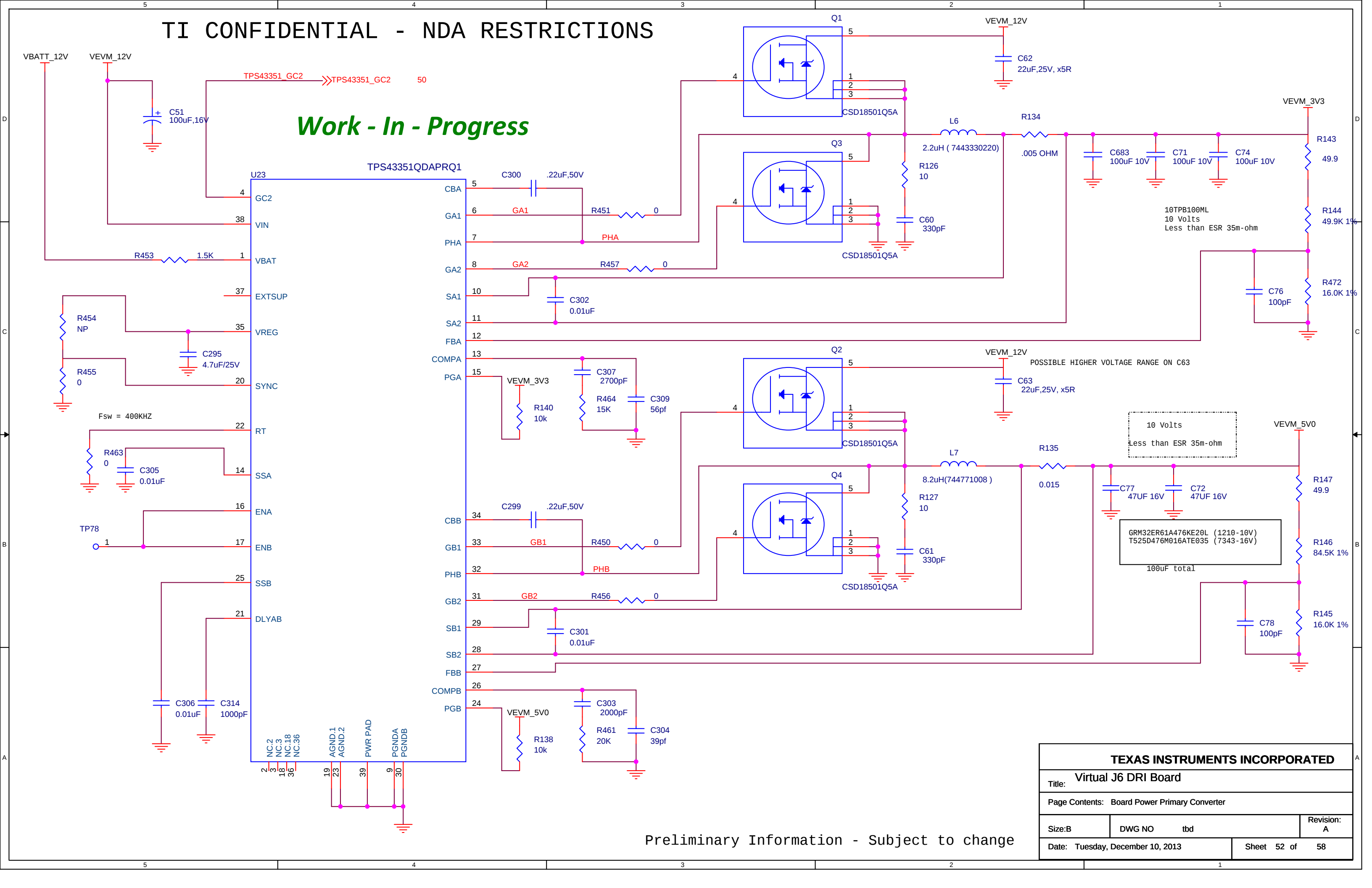
Virtual J6 DRI Board

Page Contents: Board Power Primary Converter

Size: B DWG NO tbd Revision: A

Date: Tuesday, December 10, 2013 Sheet 52 of 58

Preliminary Information - Subject to change

[illegible][illegible][illegible]

TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

The schematic diagram illustrates a 3V3 switch supply circuit using the TPS22965DSG (U92). The circuit is powered by VEVM_3V3 and VEVM_5V0. The input to the TPS22965DSG is connected to VIN.1 and VIN.2. The output is connected to VOUT.1 and VOUT.2. The ON pin is connected to PMIC_GPIO_4_6. The VBIAS pin is connected to a 1.2 volt input. The CT pin is connected to a capacitor C318 (220pF 50V). The GND pin is connected to ground. The VOUT.1 pin is connected to a capacitor C319 (NP). The VOUT.2 pin is connected to a diode E8 (NFM21PC474R1C3D). The VOUT.1 pin is also connected to a diode E11 (NFM21PC474R1C3D). The output of the circuit is connected to VDDSHV and VDAC_3V3. A resistor R473 (10K) is connected to the ON pin. A resistor R35 is connected to the VBIAS pin. A resistor R0 is connected to the VBIAS pin. A capacitor C318 (220pF 50V) is connected to the CT pin. A capacitor C319 (NP) is connected to the VOUT.1 pin. A diode E8 (NFM21PC474R1C3D) is connected to the VOUT.2 pin. A diode E11 (NFM21PC474R1C3D) is connected to the VOUT.1 pin. The circuit is labeled with various components and their values, including R473 (10K), R35, R0, C318 (220pF 50V), C319 (NP), E8 (NFM21PC474R1C3D), and E11 (NFM21PC474R1C3D). The circuit is also labeled with various power sources and signals, including VEVM_3V3, VEVM_5V0, PMIC_GPIO_4_6, VDDSHV, and VDAC_3V3. The circuit is labeled with the part number TPS22965DSG and the manufacturer TI.

43 PMIC_GPIO_4_6

VEVM_3V3

VEVM_5V0

1.2 volt input

R473 10K

R35

R0

U92

VIN.1

VIN.2

ON

VBIAS

CT

GND

VOUT.1

VOUT.2

PWR_PAD

TPS22965DSG

C318 220pF 50V

C319 NP

E8 NFM21PC474R1C3D

E11 NFM21PC474R1C3D

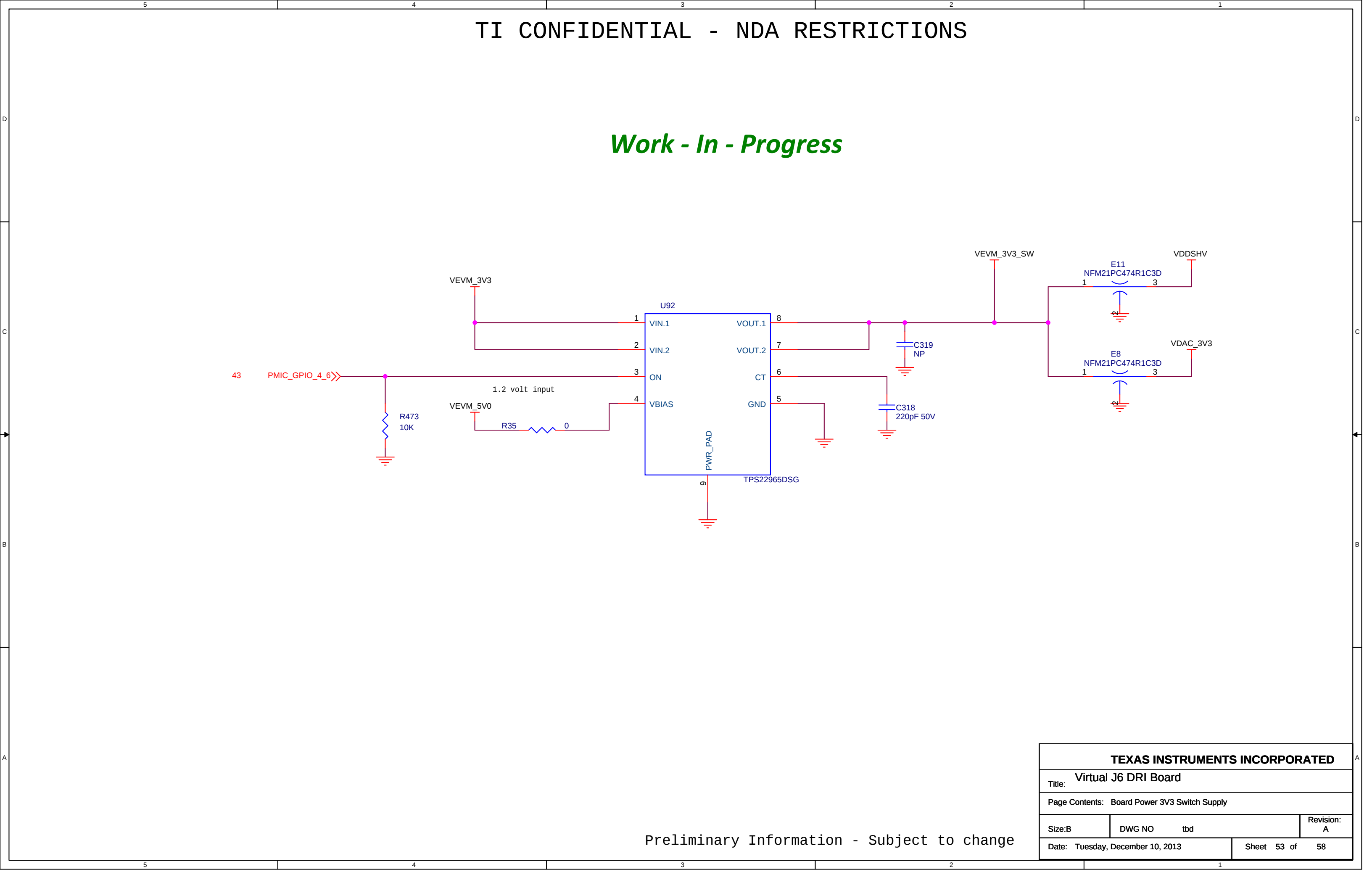
VEVM_3V3_SW

VDDSHV

VDAC_3V3

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power 3V3 Switch Supply			
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Preliminary Information - Subject to change



TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

43 PMIC_GPIO_4_6

VEVM_3V3

VEVM_5V0

1.2 volt input

R473 10K

R35 0

U92

TPS22965DSG

VIN.1

VIN.2

ON

VBIAS

VOUT.1

VOUT.2

CT

GND

PWR_PAD

VEVM_3V3_SW

C319 NP

C318 220pF 50V

E11 NFM21PC474R1C3D

E8 NFM21PC474R1C3D

VDDSHV

VDAC_3V3

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power 3V3 Switch Supply			
Size: B	DWG NO	tbd	Revision: A
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Preliminary Information - Subject to change

TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

43 PMIC_GPIO_4_6

VEVM_3V3

VEVM_5V0

1.2 volt input

R473 10K

R35 0

U92

VIN.1

VIN.2

ON

VBIAS

VOUT.1

VOUT.2

CT

GND

PWR_PAD

TPS22965DSG

VEVM_3V3_SW

C319 NP

C318 220pF 50V

E11 NFM21PC474R1C3D

E8 NFM21PC474R1C3D

VDDSHV

VDAC_3V3

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power 3V3 Switch Supply			
Size: B	DWG NO	tbd	Revision: A
Date: Tuesday, December 10, 2013	Sheet 53 of		58

Preliminary Information - Subject to change

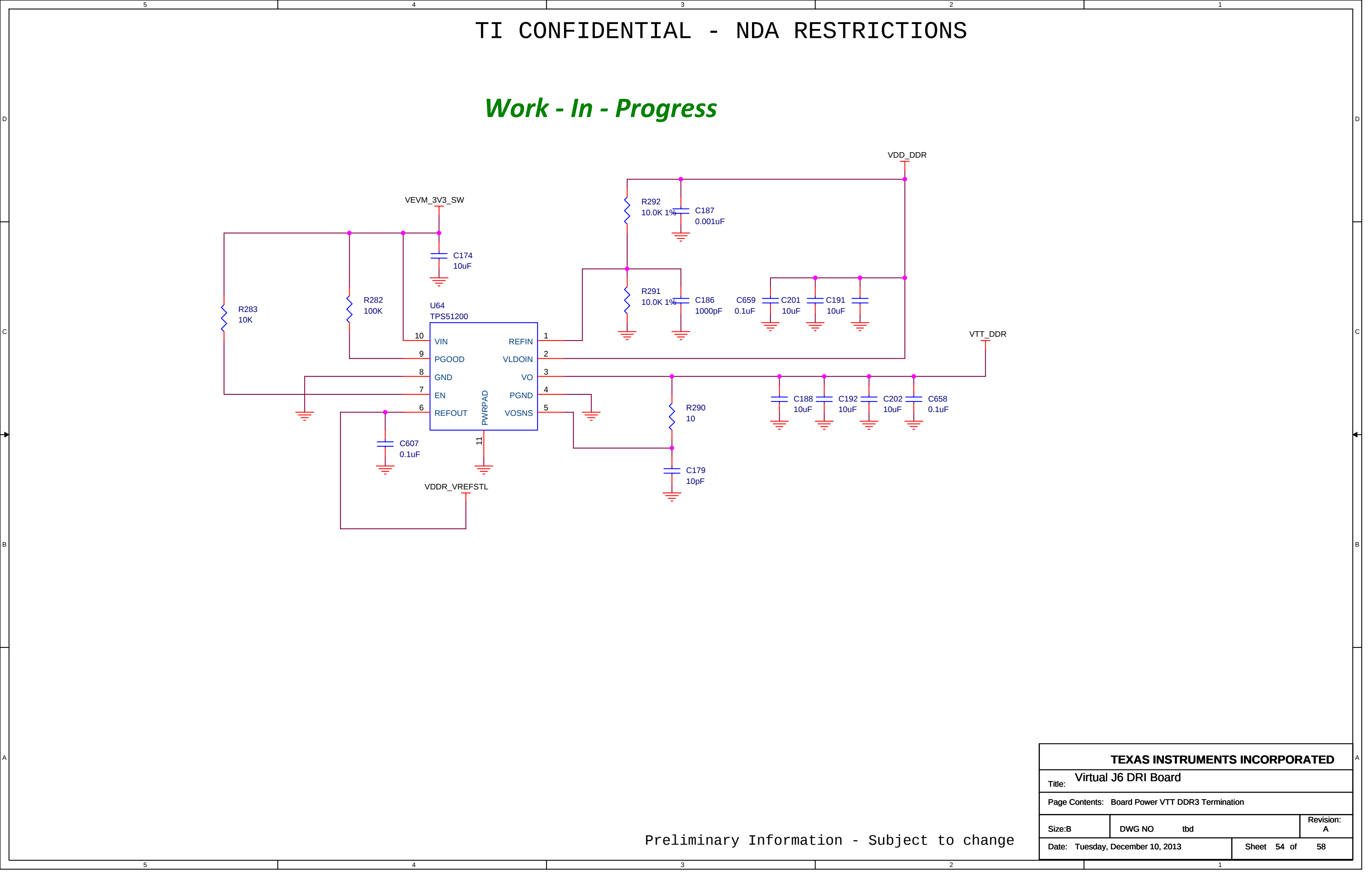
TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

The schematic diagram illustrates the power and termination circuitry for the Board Power VTT DDR3. The central component is the TPS51200 voltage regulator (U64). Its VIN pin is connected to the VDD_DDR plane through a 10K resistor (R283) and a 100K resistor (R282). The PGOOD pin is connected to the VDD_DDR plane through a 100K resistor (R282). The GND pin is connected to ground. The EN pin is connected to ground through a 0.1uF capacitor (C607). The REFOUT pin is connected to the VDDR_VREFSTL plane. The PWRPAD pin is connected to ground. The REFIN pin is connected to the VDD_DDR plane through a 10.0K 1% resistor (R292) and a 0.001uF capacitor (C187). The VLDOIN pin is connected to the VDD_DDR plane through a 10.0K 1% resistor (R291) and a 1000pF capacitor (C186). The VO pin is connected to the VTT_DDR plane through a 10 ohm resistor (R290) and a 10pF capacitor (C179). The PGND pin is connected to ground. The VOSNS pin is connected to ground. The VDD_DDR plane is connected to the VTT_DDR plane through a 0.1uF capacitor (C659) and four 10uF capacitors (C201, C191, C188, C192). The VTT_DDR plane is connected to ground through four 10uF capacitors (C201, C191, C188, C192) and a 0.1uF capacitor (C658).

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power VTT DDR3 Termination			
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Preliminary Information - Subject to change



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VDD_DDR

VTT_DDR

VDDR_VREFSTL

U64
TPS51200

R283
10K

R282
100K

R292
10.0K 1%

R291
10.0K 1%

R290
10

C174
10uF

C607
0.1uF

C187
0.001uF

C186
1000pF

C659
0.1uF

C201
10uF

C191
10uF

C188
10uF

C192
10uF

C202
10uF

C658
0.1uF

C179
10pF

VEVM_3V3_SW

VDD_DDR

VTT_DDR

VDDR_VREFSTL

REFIN

VLDOIN

VO

PGND

VOSNS

VIN

PGOOD

GND

EN

REFOUT

PWRPAD

1

2

3

4

5

6

7

8

9

10

11

Size:B

DWG NO

tbd

Revision:
A

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TI CONFIDENTIAL - NDA RESTRICTIONS

Work - In - Progress

VDD_DDR

VTT_DDR

VDDR_VREFSTL

U64
TPS51200

R283
10K

R282
100K

R292
10.0K 1%

R291
10.0K 1%

R290
10

C174
10uF

C607
0.1uF

C187
0.001uF

C186
1000pF

C659
0.1uF

C201
10uF

C191
10uF

C188
10uF

C192
10uF

C202
10uF

C658
0.1uF

C179
10pF

VEVM_3V3_SW

VDD_DDR

VTT_DDR

VDDR_VREFSTL

REFIN

VLDOIN

VO

PGND

VOSNS

EN

PGOOD

GND

REFOUT

PWRPAD

10

9

8

7

6

11

5

4

3

2

1

Size:B

DWG NO

tbd

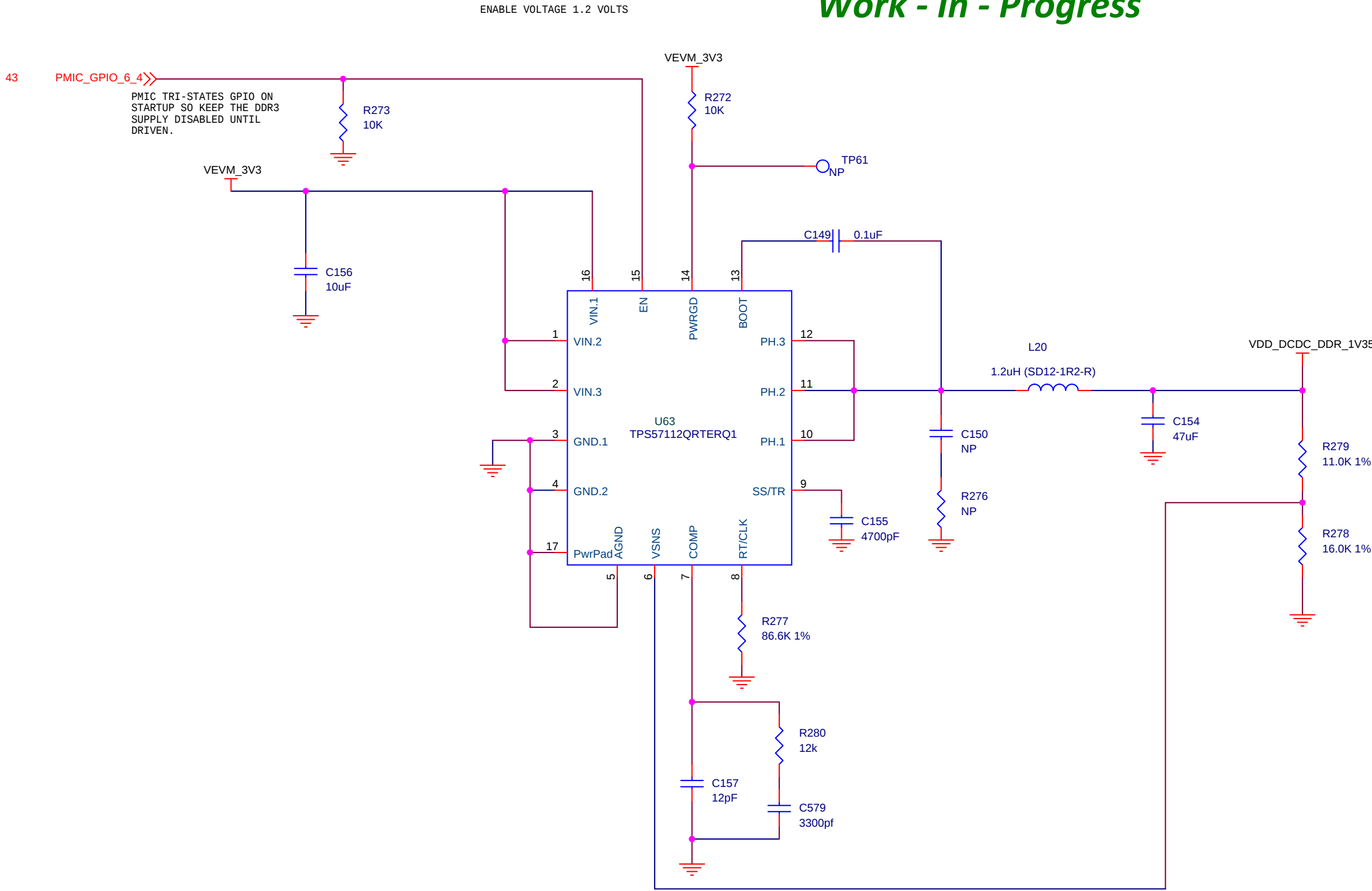
Revision:
A

Date: Tuesday, December 10, 2013

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Work - In - Progress

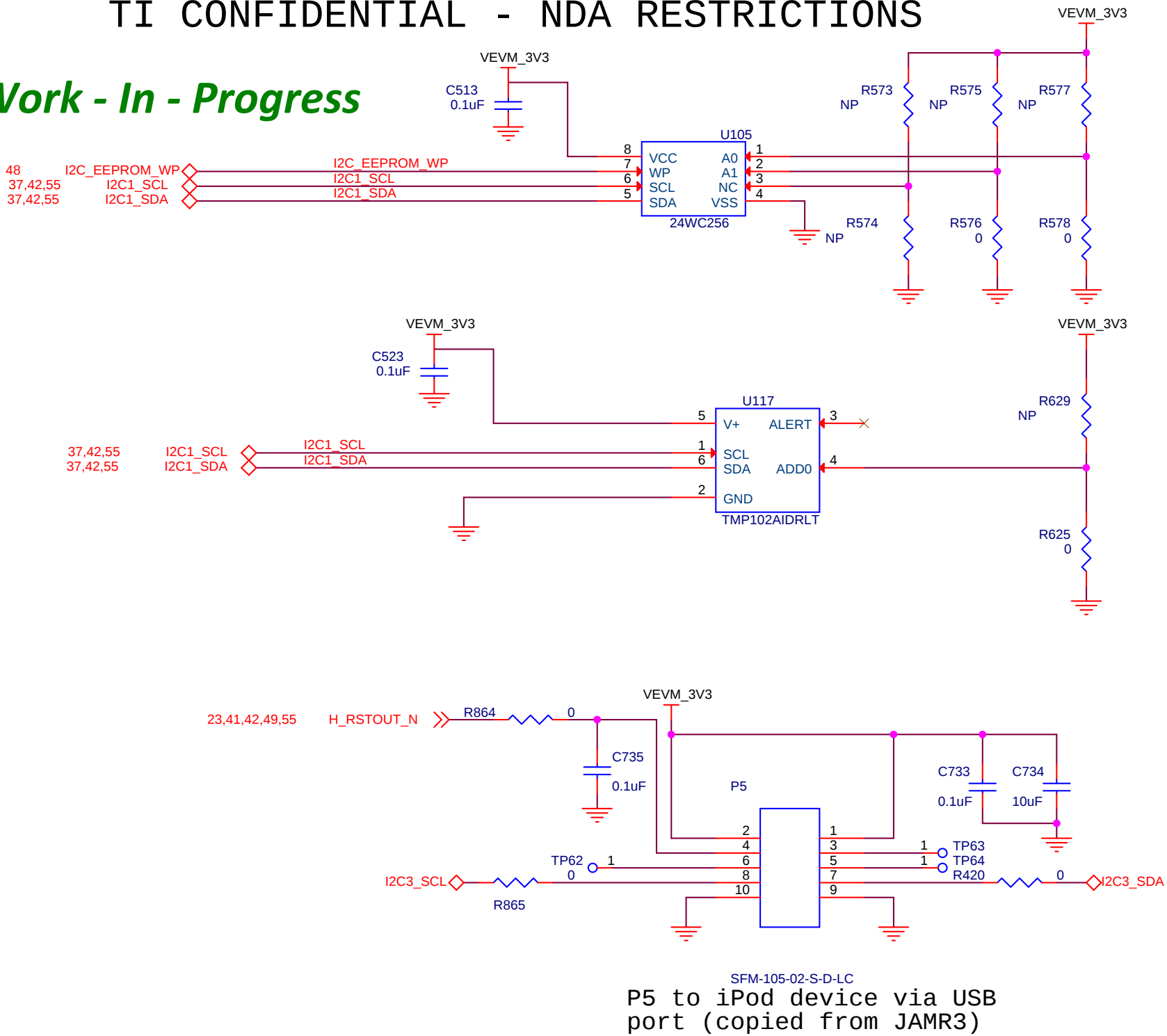


Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Board Power 1V35 DDR3 Core			
Size:B	DWG NO	tbd	Revision: A
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Work - In - Progress



P5 to iPod device via USB
port (copied from JAMR3)

Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: BD EEPROM Temperature Sensor IPOD I/F			
Size: B	DWG NO	tbd	Revision: A
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PCB Matched Group = H_QSPI_xxx

Mode = SCK for single commands
Max Clk = 133MHz
Mode = SCK for dual & quad commands
Max Clk = 104MHz

PCB Matched Group = H_MMC1_xxx

Mode = SDR104
Max Clk = 192MHz
Max Data = 96Mbps

Work - In - Progress

See DRA75x_74x Data Manual, Section 8.4.2
QSPI Board Design & Layout Guidelines

8.4.2 QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

- The qspi1_sclk output signal must be looped back into the qspi1_rtclock input.
- The signal propagation delay from the qspi1_sclk ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the qspi1_rtclock ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the qspi1_rtclock ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the qspi1_sclk signal to the series terminators (R2 = 10 Ω) near the QSPI device must be < 450pS (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-29.

PCB Matched Group = H_MMC2_xxx

Mode = HS200
Max Clk = 192MHz
Max Data = 96Mbps

SPRS857F –DECEMBER 2012–REVISED SEPTEMBER 2013

- Propagation delays and matching:
 - A to C = C to D = E to F.
 - Matching skew: < 60pS
 - A to B < 450pS
 - B to C = as small as possible (<60pS)

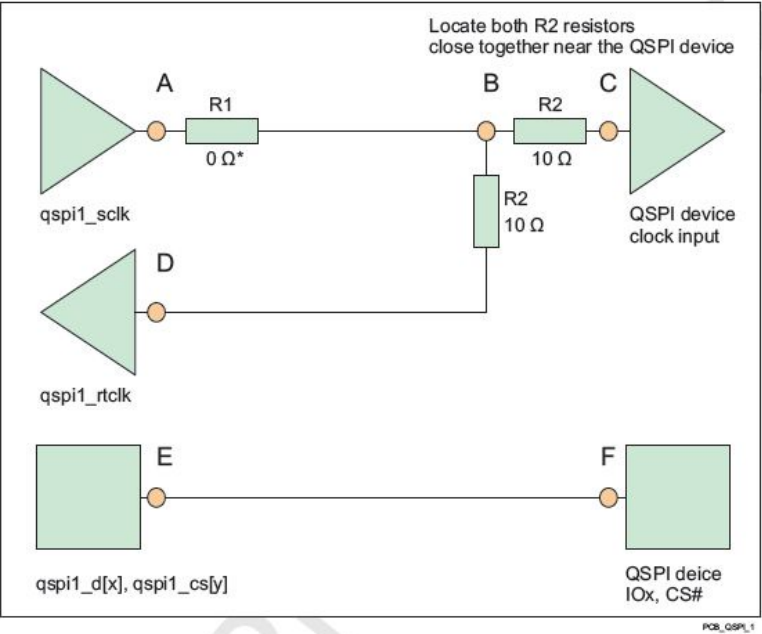


Figure 8-29. QSPI Interface High Level Schematic

NOTE

*0 Ω resistor (R1), located as close as possible to the qspi1_sclk pin, is placeholder for fine-tuning if needed.

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: PCB Design Notes			
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Rev	Date	Author	Notes
B	12/10/2013	Bill McCracken	Reduced Dcaps on VDD_CORE, VDD_MPU, VDD_DDR & VDD_DSPEVE_IVA_GPU power rails to align with Power Integrity modelnig results for optimizing Dcap Schemes.
D			
C			
B			
A			

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Preliminary Information - Subject to change

TEXAS INSTRUMENTS INCORPORATED			
Title: Virtual J6 DRI Board			
Page Contents: Revision History			
Size:C	DWG NO	tbd	Revision: A
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